3.1 BASIC CONCEPT OF VOLTAGE-SOURCED CONVERTER

Discussion of FACTS Controller concepts in Chapter 1 conveyed that the voltage-sourced converter is the building block of STATCOM, SSSC, UPFC, IPFC, and some other Controllers. Therefore, this converter is generically discussed in this chapter.

It was explained in Chapter 2 that the so-called conventional thyristor device has only the turn-on control; its turn-off depends on the current coming to zero as per circuit and system conditions. Devices such as the Gate Turn-Off Thyristor (GTO), Integrated Gate Bipolar Transistor (IGBT), MOS Turn-off Thyristor (MTO), and Integrated Gate-Commutated Thyristors (IGCT), and similar devices have turn-on and turn-off capability. These devices (referred to as turn-off devices) are more expensive and have higher losses than the thyristors without turn-off capability; however, turn-off devices enable converter concepts that can have significant overall system cost and performance advantages. These advantages in principle result from the converters, which are self-commutating as against the line-commutating converters. Compared to the self-commutating converter, the line-commutating converter must have an ac source connected to the converter, it consumes reactive power, and suffers from occasional commutation failures in the inverter mode of operation. Therefore, unless a converter is required to function in the two lagging-current quadrants only (consuming reactive power while converting active power), converters applicable to FACTS Controllers would be of the self-commutating type. There are two basic categories of self-commutating converters:

1. Current-sourced converters in which direct current always has one polarity, and the power reversal takes place through reversal of dc voltage polarity.
2. Voltage-sourced converters in which the dc voltage always has one polarity, and the power reversal takes place through reversal of dc current polarity.

Conventional thyristor-based converters, being without turn-off capability, can only be current-sourced converters, whereas turn-off device-based converters can be of either type.
For reasons of economics and performance, voltage-sourced converters are often preferred over current-sourced converters for FACTS applications, and in this chapter various self-commutating voltage-sourced converter concepts, which form the basis of several FACTS Controllers, will be discussed.

Since the direct current in a voltage-sourced converter flows in either direction, the converter valves have to be bidirectional, and also, since the dc voltage does not reverse, the turn-off devices need not have reverse voltage capability; such turn-off devices are known as asymmetric turn-off devices. Thus, a voltage-sourced converter valve is made up of an asymmetric turn-off device such as a GTO [as shown in Figure 3.1(a)] with a parallel diode connected in reverse. Some turn-off devices, such as the IGBTs and IGCTs, may have a parallel reverse diode built in as part of a complete integrated device suitable for voltage-sourced converters. However, for high power converters, provision of separate diodes is advantageous. In reality, there would be several turn-off device-diode units in series for high-voltage applications. In general,

**Figure 3.1** Basic principles of voltage-sourced converters: (a) Valve for a voltage-sourced converter; (b) Voltage-sourced converter concept; (c) Single-valve operation.
the symbol of one turn-off device with one parallel diode, as shown in Figure 3.1(a), will represent a valve of appropriate voltage and current rating required for the converter.

Within the category of voltage-sourced converters, there are also a wide variety of converter concepts. The ones relevant to FACTS Controllers are described in this chapter. There are some converter topologies that are suitable for supplying and consuming reactive power only and not for converting active power; they are not discussed in this chapter.

Figure 3.1(b) shows the basic functioning of a voltage-sourced converter. The internal topology of converter valves is represented as a box with a valve symbol inside. On the dc side, voltage is unipolar and is supported by a capacitor. This capacitor is large enough to at least handle a sustained charge/discharge current that accompanies the switching sequence of the converter valves and shifts in phase angle of the switching valves without significant change in the dc voltage. For the purposes of discussion in this chapter, the dc capacitor voltage will be assumed constant. It is also shown on the dc side that the dc current can flow in either direction and that it can exchange dc power with the connected dc system in either direction. Shown on the ac side is the generated ac voltage connected to the ac system via an inductor. Being an ac voltage source with low internal impedance, a series inductive interface with the ac system (usually through a series inductor and/or a transformer) is essential to ensure that the dc capacitor is not short-circuited and discharged rapidly into a capacitive load such as a transmission line. Also an ac filter may be necessary (not shown) following the series inductive interface to limit the consequent current harmonics entering the system side.

Basically a voltage-sourced converter generates ac voltage from a dc voltage. It is, for historical reasons, often referred to as an inverter, even though it has the capability to transfer power in either direction. With a voltage-sourced converter, the magnitude, the phase angle and the frequency of the output voltage can be controlled.

In order to further explain the principles, Figure 3.1(c) shows a diagram of a single-valve operation. DC voltage, \( V_d \), is assumed to be constant, supported by a large capacitor, with the positive polarity side connected to the anode side of the turn-off device. When turn-off device 1 is turned on, the positive dc terminal is connected to the ac terminal, \( A \), and the ac voltage would jump to \( +V_d \). If the current happens to flow from \( +V_d \) to \( A \) (through device 1), the power would flow from the dc side to ac side (inverter action). However, if the current happens to flow from \( A \) to \( +V_d \) it will flow through diode 1' even if the device 1 is so called turned on, and the power would flow from the ac side to the dc side (rectifier action). Thus, a valve with a combination of turn-off device and diode can handle power flow in either direction, with the turn-off device handling inverter action, and the diode handling rectifier action. This valve combination and its capability to act as a rectifier or as an inverter with the instantaneous current flow in positive (ac to dc side) or negative direction, respectively, is basic to voltage-sourced converter concepts.

### 3.2 SINGLE-PHASE FULL-WAVE BRIDGE CONVERTER OPERATION

Although FACTS Controllers will generally utilize three-phase converters, a single-phase, full-wave bridge converter may also be used in some designs. In any case, it is
important to first understand the operation of a single-phase bridge converter and operation of a phase-leg to further understand the principles of voltage-sourced converters.

Figure 3.2(a) shows a single-phase full-wave bridge converter consisting of four valves, (1–1’) to (4–4’), a dc capacitor to provide stiff dc voltage, and two ac connection points, a and b. The designated valve numbers represent their sequence of turn-on and turn-off. The dc voltage is converted to ac voltage with the appropriate valve turn-on, turn-off sequence as explained below.

As shown by the first waveform of Figure 3.2(b), with turn-off devices 1 and 2 turned on, voltage \( v_{ab} \) becomes \( +V_d \) for one half-cycle, and, with 3 and 4 turned on and devices 1 and 2 turned off, \( v_{ab} \) becomes \( -V_d \) for the other half-cycle. This voltage waveform occurs regardless of the phase angle, magnitude and waveform of the ac current flow. The ac current is the result of interaction of the converter generated ac voltage with the ac system voltage and impedance. For example, suppose that the current flow from the ac system, as shown by the second waveform, is a sinusoidal waveform \( l_{ab} \), angle \( \theta \), leading with respect to the square-wave voltage waveform. Starting from instant \( t_1 \), it is seen from the circuit and the waveform that:

1. From instant \( t_1 \) to \( t_2 \), with turn-off devices 1 and 2 on and 3 and 4 off, \( v_{ab} \) is positive and \( l_{ab} \) is negative. The current flows through device 1 into ac phase a, and then out of ac phase b through device 2, with power flow from dc to ac (inverter action).

2. From instant \( t_2 \) to \( t_3 \), the current reverses, i.e., becomes positive, and flows through diodes 1’ and 2’ with power flow from ac to dc (rectifier action). Note that during this interval, although devices 1 and 2 are still on and voltage \( v_{ab} \) is \( +V_d \), devices 1 and 2 cannot conduct in a reverse direction. In reality, devices 1 and 2 are ready to turn on by turn-on pulses when required by the direction of actual current flow.

3. From instant \( t_3 \) to \( t_4 \), devices 1 and 2 are turned off and devices 3 and 4 are turned on, thereby \( v_{ab} \) becomes negative while \( l_{ab} \) is still positive. The current now flows through devices 3 and 4 with power flow from dc to ac (inverter action).

4. From instant \( t_4 \) to \( t_5 \), with devices 3 and 4 still on, and 1 and 2 off, and \( v_{ab} \) negative, current \( l_{ab} \) reverses and flows through diodes 3’ and 4’ with power flow from ac to dc (rectifier action).

From instant \( t_5 \), the cycle starts again as from \( t_1 \), with devices 1 and 2 turned on and 3 and 4 turned off. Table 3.1 summarizes the four operating modes in a cycle.

Figure 3.2(b) also shows the waveform of current flow \( i_d \) in the dc bus with the positive side flowing from ac to dc (rectifier action), and the negative side flowing from dc to ac (inverter action). Clearly the average dc current is negative. The current \( i_d \) contains the dc current and the harmonics. The dc current must flow into the dc system and for a large dc capacitor, virtually all of the harmonic current will flow through the capacitor. Being a single-phase, full-wave bridge, the dc harmonics have an order of \( 2k \), where \( k \) is an integer, i.e., 2nd, 4th, 6th, . . ., all of the even harmonics.

Voltage across valve 1-1’ is shown as the last waveform in Figure 3.2(b).

The relationship between ac voltage and current phasors is shown in Figure 3.2(c), showing power flow from ac to dc with a lagging power factor.
Figure 3.2 Single-phase, full-wave, voltage-sourced converter: (a) Single-phase, full-wave circuit; (b) Operation waveform; (c) Phase relationship between current and voltage.
### Table 3.1  Four Operating Modes in One Cycle of a Single-Phase Converter

<table>
<thead>
<tr>
<th>Devices</th>
<th>$V_{ab}$</th>
<th>Current Flow</th>
<th>Conducting Devices</th>
<th>Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 &amp; 2 on, 3 &amp; 4 off</td>
<td>Positive</td>
<td>Negative</td>
<td>1 &amp; 2</td>
<td>Inverter:</td>
</tr>
<tr>
<td>1 &amp; 2 on, 3 &amp; 4 off</td>
<td>Positive</td>
<td>Positive</td>
<td>1' &amp; 2'</td>
<td>Rectifier:</td>
</tr>
<tr>
<td>1 &amp; 2 off, 3 &amp; 4 on</td>
<td>Negative</td>
<td>Positive</td>
<td>3 &amp; 4</td>
<td>Inverter:</td>
</tr>
<tr>
<td>1 &amp; 2 off, 3 &amp; 4 on</td>
<td>Negative</td>
<td>Negative</td>
<td>3' &amp; 4'</td>
<td>Rectifier:</td>
</tr>
</tbody>
</table>

### 3.3 Single Phase-Leg (Pole) Operation

Now consider operation of just one-leg (single-pole) circuit shown in Figure 3.3, in which the capacitor is split into two series-connected halves with the neutral point of the ac side connected to the midpoint $N$ of the dc capacitor. With the two turn-off devices alternately closing/opening, the ac voltage waveform is a square wave with peak voltage of $V_d/2$. Note that when two phase-legs are operated in a full-wave bridge mode, Figure 3.2(b), the ac square wave is the sum of the two halves of Figure 3.3(b), giving a peak voltage of $V_d$. In a full-wave circuit, the neutral connection is no longer needed, because the current has a return path through the other phase-leg.

It should now be obvious that:

1. AC current and voltage can have any phase relationship, that is, the converter phase angle between voltage and current can cover all four quadrants, i.e., act as a rectifier or an inverter with leading or lagging reactive power. This

![Figure 3.3](image-url)
assumes that there is a dc and an ac system connected on the two sides of the converter, as in Figure 3.1(b), to exchange real power. If the converter is used for reactive power only then there is no need for the dc system and the converter will terminate at the dc capacitor.

2. The active and reactive power can be independently controlled with control of magnitude and angle of the converter generated ac voltage with respect to the ac current.

3. Diodes carry out instantaneous rectifier function, and turn-off devices carry out instantaneous inverter function. Of course, each ac cycle is made up of periods of rectifier and inverter actions in accordance with the phase angle, and the average current determines the net power flow and hence the net rectifier or inverter operation. When the converter operates as a rectifier with unity power factor, only diodes are involved with conduction, and when it operates as an inverter with unity power factor, only turn-off devices are involved in conduction.

4. When any turn-off device turns off, the ac bus current is not actually interrupted at all, but is transferred from a turn-off device to a diode when the power factor is not unity, and to another turn-off device when power factor is unity.

5. Turn-off devices 1 and 4 (or turn-off devices 2 and 3) in the same phase-leg are not turned on simultaneously. Otherwise this would cause a "shoot-through" (short circuit) of the dc side and a very fast discharge of the dc capacitor through the shorted phase-leg, which will destroy the devices in that phase-leg. In a phase-leg, when one turn-off device is on, the other is off. The gate control is arranged to ensure that only one of the two devices in a phase-leg receives a turn-on pulse, and that the current in the other device was indeed zero. Regardless, sensing and protection means are provided, usually to ensure safe shutdown of the converter.

6. Each phase-leg is independently capable of operating at any frequency or timing with the two valves in a leg alternately switching.

7. In principle, any number of phase-legs can be connected in parallel and each operated independently although being connected to the ac system, there is a need to have appropriate sequence and system interface through transformers in order to achieve the desired converter performance.

8. It is important to note that turn-on and turn-off of the turn-off devices establish the voltage waveform of the ac bus voltage in relation to the dc voltage, and do not necessarily conduct current if the direction of current flow results in a corresponding diode to carry the current.

Operation of each phase leg is further discussed in Section 3.6.

3.4 SQUARE-WAVE VOLTAGE HARMONICS FOR A SINGLE-PHASE BRIDGE

The square wave, shown in Figure 3.2(b) as the ac voltage $v_{ab}$, has substantial harmonics in addition to the fundamental. These harmonics are of the order $2n \pm 1$ where $n$ is an integer, i.e., 3rd, 5th, 7th ... The magnitude of the 3rd is 1/3rd of the fundamental, the 5th is 1/5th of fundamental, and so on.

As mentioned earlier, an inductive interface with the ac system (usually through an inductor and/or transformer) is essential to ensure that the dc capacitor does not
discharge rapidly into a capacitive load such as a transmission line but it is also essential to reduce the consequent harmonic current flow. Generally, an ac filter would be necessary following the inductive interface to limit the consequent current harmonics on the system side although the filters will only increase the harmonic current in the converter itself. It would therefore be preferable if the converter generated less harmonics so that it does not require ac filters in the first place.

Integration of the waveform in Figure 3.2(b) gives the rms value of the square-wave ac voltage with a peak voltage of $V_d$:

$$V_{ab} = \sqrt{\frac{1}{\pi} \int_{-\pi/2}^{\pi/2} V_d^2 \, dt} = V_d$$

which includes the fundamental and the harmonics. The fundamental and individual harmonics are given by

$$v = \frac{4}{\pi} (V_d) \left[ \cos \omega t - \frac{1}{3} \cos 3\omega t + \frac{1}{5} \cos 5\omega t - \frac{1}{7} \ldots \right]$$

which gives

$$v_n = \frac{4}{\pi} (V_d) \left[ \frac{1}{n} \cos n\omega t \right]$$

for $n = 1, 3, 5, 7 \ldots$

and its rms value given by

$$V_n = \frac{1}{n} \frac{2\sqrt{2}}{\pi} V_d$$

Thus, the rms fundamental component of a square wave ac voltage $v_{ab}$ is

$$V_1 = \frac{2\sqrt{2}}{\pi} V_d = 0.9 V_d$$

and the magnitude of each voltage harmonic is $1/n$th of the fundamental. These voltage harmonics will cause current harmonics to flow into the system, the magnitude of each determined by the system impedance. It is therefore essential to provide an inductive interface followed by shunt capacitive filters if necessary. Since for the $n$th harmonic the voltage is $1/n$th the fundamental voltage and the inductive impedance is $n$ times the fundamental frequency impedance, it follows that lower frequency harmonics are the biggest concern.

### 3.5 THREE-PHASE FULL-WAVE BRIDGE CONVERTER

#### 3.5.1 Converter Operation

Figure 3.4(a) shows a three-phase, full-wave converter with six valves, (1–1’) to (6–6’). The designated order 1 to 6 represents the sequence of valve operation in time. It consists of three phase-legs, which operate in concert, 120 degrees apart. The three phase-legs operate in a square wave mode, in accordance with the square wave mode described in the section above and with reference to Figure 3.3. Each valve alternately closes for 180 degrees as shown by the waveforms $u_a$, $u_b$, and $u_c$ in Figure 3.4(b). These three square-wave waveforms are the voltages of ac buses a, b, and c.
with respect to a hypothetical dc-capacitor midpoint, $N$, with peak voltages of $+V_d/2$ and $-V_d/2$. The three phase legs have their timing 120 degrees apart with respect to each other in what amounts to a 6-pulse converter operation. Phase-leg 3–6 switches 120 degrees after phase-leg 1–4, and phase-leg 5–2 switches 120 degrees after phase-leg 3–6, thus completing the cycle as shown by the valve close-open sequence.

Figure 3.4(b) also shows the three phase-to-phase voltages, $v_{ab}$, $v_{bc}$, and $v_{ca}$, where $v_{ab} = v_a - v_b$, $v_{bc} = v_b - v_c$, and $v_{ca} = v_c - v_a$. It is interesting to note that these phase-to-phase voltages have 120 degrees pulse-width with peak voltage magnitude of $V_d$. The periods of 60 degrees, when the phase-to-phase voltages are zero, represent the condition when two valves on the same side of the dc bus are closed on their dc bus.

For example, the waveform for $v_{ab}$ shows voltage $V_d$ when turn-off device 1 connects ac bus $a$ to the dc bus $+V_d/2$, and turn-off device 6 connects ac bus $b$ to the dc bus $-V_d/2$, giving a total voltage $v_{ab} = v_a - v_b = V_d$. It is seen that 120 degrees later, when turn-off device 6 is turned off and turn-off device 3 is turned on, both ac buses, $a$ and $b$, become connected to the same dc bus $+V_d/2$, giving zero voltage between buses $a$ and $b$. Another 60 degrees later, as turn-off device 1 turns off, and turn-off device 4 connects bus $a$ to $-V_d/2$, $v_{ab}$ becomes $-V_d$. Another 120 degrees later, turn-off device 3 turns off, and turn-off device 6 connects bus $b$ to $-V_d/2$, giving $v_{ab} = 0$. The cycle is completed when, after another 60 degrees turn-off device 4 turns off, and turn-off device 1 turns on. The other two voltages $v_{bc}$ and $v_{ca}$ have the same sequence 120 degrees apart.

As mentioned earlier, the turn-on and turn-off of the devices establish the waveforms of the ac bus voltages in relation to the dc voltage, the current flow itself is the result of the interaction of the ac voltage with the ac system. Also as mentioned earlier, each converter phase-leg can handle resultant current flow in either direction. Figure 3.4(b) shows an assumed ac current $i_a$ in phase $a$, with positive current representing current from the ac to the dc side. For simplicity, the current is assumed to have fundamental frequency only. From point $t_1$ to $t_2$, for example, phase a current is negative and has to flow through either valve 1–1’ or valve 4–4’. It is seen, when comparing the phase a voltage (top curve) with the waveform of the phase a current, that when turn-off device 4 is on and turn-off device 1 is off and the current is negative, the

![Figure 3.4 Operation of a three-phase, full-wave voltage-sourced converter: (a) Three-phase, full-wave converter; (b) AC waveforms of a three-phase, full-wave converter; (c) DC current waveforms of a three-phase, full-wave voltage-sourced converter.](image-url)
Figure 3.4 Continued
Section 3.5  Three-Phase Full-Wave Bridge Converter

Figure 3.4 Continued

current would actually flow through diode 4'. But later, say from point $t_2$ to $t_3$, when device 4 is turned off and device 1 is turned on, the negative current flows through device 1, the current having transferred from diode 4' to device 1. Figure 3.4(a) shows the current flow path during $t_1$–$t_5$; the current coming out of phase b flows through device 6, but then part of this current returns back through diode 4' into phase a, and part goes into the dc bus. The dc current returns via turn-off device 5 into phase c. At any time, three valves are conducting in a three-phase converter system. In fact only the active power part of the ac current and part of the harmonics flows into the dc side as illustrated in Figure 3.4(c) and further explained later in this section.

3.5.2 Fundamental and Harmonics for a Three-Phase Bridge Converter

It should be noted that the square wave waveforms of $v_a$, $v_b$, and $v_c$ are the phase terminal voltages with respect to the hypothetical midpoint $N$ of the dc voltage and not the neutral point of the ac side. These voltages would be phase-to-neutral ac voltages only if the ac neutral is physically connected to the midpoint of the dc voltage, in which case the converter would in effect become a series connection of two three-
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pulse three-phase half-wave converters and not a six-pulse three-phase full-wave converter.

For a square wave with amplitude of $V_{d}/2$, the instantaneous values of $v_a$, $v_b$, and $v_c$ based on Fourier analysis are given by

$$ v_a = \frac{4}{\pi} \left( \frac{V_d}{2} \right) \left[ \cos \omega t - \frac{1}{3} \cos 3\omega t + \frac{1}{5} \cos 5\omega t - \frac{1}{7} \cos 7\omega t + \ldots \right] $$

$v_b$ is obtained by replacing $\omega t$ by

$$ \left( \omega t - \frac{2\pi}{3} \right) $$

and $v_c$ is obtained by replacing $\omega t$ by

$$ \left( \omega t + \frac{2\pi}{3} \right) $$

For all the triplen harmonics (i.e., 3rd, 9th . . .), the multipliers 3, 9 . . . in the terms

$$ \cos 3 \left( \omega t \pm \frac{2\pi}{3} \right), $$

$$ \cos 9 \left( \omega t \pm \frac{2\pi}{3} \right), $$

reduce these terms to $\cos 3 \omega t$, which means that all the triplen harmonics of all three phases are in phase.

Since the ac neutral in a bridge converter is floating, it is necessary to work out phase-to-neutral voltages, which appear across the transformer secondaries. If it is assumed that the three phases are connected to a wye transformer secondary with floating neutral, then the floating neutral will acquire a potential with respect to the dc midpoint which is one-third of the sum of all three voltages of phase terminals a, b, and c. Figure 3.4 shows that $v_n$ is a square-wave of magnitude $V_{d}/6$ with three times the frequency, i.e., it has all the $3n$ harmonics of the terminal voltages.

Subtracting $v_a$ from the phase terminal voltages with respect to dc neutral give the phase voltages across the wye-connected transformer secondaries, as shown only for $v_{an}$, phase a to transformer neutral voltage in Figure 3.4(b). It consists of steps of $V_{d}/3$, a six-pulse waveform free from $3n$ harmonics. It now has harmonics of only the order of $6n \pm 1$, i.e., 5th, 7th, 11th, 13th, etc. Waveforms $v_{bn}$ and $v_{cn}$ would be the same except phase shifted by 120 degrees and 240 degrees, respectively, from $v_{an}$. Note that the ac phase-to-neutral voltages are still in phase with the ac phase to dc neutral voltages, i.e., $v_{an}$ and $v_{an}$ are in phase. The only difference between $v_{an}$ and $v_{an}$ is that $v_{an}$ is with the triplen harmonics of $v_{an}$.

$$ v_{an} = \frac{4}{\pi} \left( \frac{V_d}{2} \right) \left[ \cos \omega t + \frac{1}{5} \cos 5\omega t - \frac{1}{7} \cos 7\omega t + \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t + \ldots \right] $$

The phase-to-phase waveform $v_{ab}$ shown in Figure 3.4(b) is also a six-pulse waveform, but of different waveshape than $v_{an}$. Apart from the observation that $v_{ab}$ is a two-level voltage with 0 or $V_d$ and $v_{an}$ is a three-level voltage with levels of 0, $1/3 V_d$, and $2/3 V_d$, comparison of waveforms $v_{ab}$ and $v_{an}$ shows that the two are phase shifted and $v_{ab}$ is larger than $V_{an}$. Being phase-to-phase voltage, fundamental component of $v_{ab}$ is phase shifted by $30^\circ$, and its amplitude is $\sqrt{3}$ times the $v_{an}$. 
The rms value of the phase-to-phase voltage (120 degrees, square wave with an amplitude of \( V_a \)) is given by

\[
V = \sqrt{\frac{1}{\pi} \int_{-\pi/3}^{\pi/3} V_d^2 \, d\omega t} = \sqrt{2} * \frac{V_d}{\sqrt{3}} = 0.816V_d
\]

The value of the fundamental and harmonic components of the phase-to-phase voltage is given by

\[
v_{ab} = \frac{2\sqrt{3}}{\pi} \frac{V_d}{n} \left[ \cos \omega t - \frac{1}{5} \cos 5\omega t + \frac{1}{7} \cos 7\omega t - \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t - \ldots \right]
\]

The rms value of the fundamental is given by

\[
V_f = \frac{\sqrt{6}}{\pi} V_d = 0.78V_d
\]

compared to the total rms value (including harmonics) of 0.816 \( V_d \).

Individual harmonic voltage is given by

\[
V_n = V_f/n
\]

The value of fundamental and harmonic component of the phase-to-neutral voltage is given by

\[
v_{an} = \frac{2}{\pi} \frac{V_d}{n} \left[ \cos \omega t + \frac{1}{5} \cos 5\omega t - \frac{1}{7} \cos 7\omega t - \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t + \ldots \right]
\]

Note that both \( v_{ab} \) and \( v_{an} \) are defined above with their own zero reference and in fact the two are 30 degrees out of phase.

Figure 3.4(c) shows the dc side current waveforms. Consider first the waveform \( i_a \) for current in phase a, shown in Figure 3.4(b), this current flows through the phase-leg with valves 1–1′ and 4–4′. Reversing the waveform sections of the valve 4–4′ gives the dc current contribution of the phase-leg a, to the total current in the dc bus on converter side of the dc capacitors, as shown by the top waveform in Figure 3.4(c). Contribution of current from the other two phase-legs is shown by the next two waveforms in Figure 3.4(c). Adding up the three currents gives the total dc current \( i_d \) in the dc bus, as shown by the third waveform of Figure 3.4(c). It consists of direct current component and harmonics of the order of \( n = 6k \), i.e., 6th, 12th, 18th, \ldots. The direct current component of this current is given by:

\[
i_d = (3\sqrt{2}/\pi)I \cos \theta = 1.35 I \cos \theta
\]

where \( I \) is the rms ac phase current and \( \theta \) is the power factor angle. The current is maximum at 1.35 \( I \), when power factor is unity and changes from +1.35 \( I \) to −1.35 \( I \), and vice versa, as the angle changes from full rectification to inversion of power.

\( N \)th-harmonic current is at its minimum when power factor is unity and corresponds to

\[
I_n/I_{dn} = \sqrt{2}/(n^2 - 1), \text{ where } I_{dn} \text{ is the peak value of the dc bus current}
\]

and increases to maximum when power factor is zero and corresponds to

\[
I_n/I_{dn} = \sqrt{2n}/(n^2 - 1)
\]
The higher the \( n \), the lower is the harmonic amplitude, and clearly the three-phase, full-wave converter has much lower harmonics than the single-phase, full-wave converter because of the elimination of low-order and other harmonics, particularly the second harmonic. However, even in a six-pulse operation, the second harmonic will reappear during ac voltage unbalances, and the system needs to be designed to suppress and/or ride through low frequency harmonics during ac system faults and other reasons for system unbalance.

3.6 SEQUENCE OF VALVE CONDUCTION PROCESS IN EACH PHASE-LEG

It is necessary to discuss the operation of each phase-leg in greater detail, in order to relate to a variety of converter topologies.

It is clear from the discussion in the sections above, that each phase-leg operates independently, and involves alternate turn-on and turn-off of the devices. For instantaneous current (power) flow from ac to dc, the current flows through the diodes, and, for instantaneous current (power) flow from dc to ac, the current flows through the turn-off devices. Figure 3.3 shows an ac voltage waveform of one phase-leg (with respect to the dc midpoint), with a varying phase angle with respect to an assumed sinusoidal current flow. It is not important to be concerned about where the current is going on the ac or dc sides, because in a complete circuit there will be other phase-legs and ac and dc system connections for a complete current loop.

The ac voltage waveform represents at the start an inverter with a unity power factor for a one-cycle segment. It then makes a phase delay of 60 degrees to show the operation for the next one cycle of inverter operation with phase delay of 60 degrees from the unity power factor. This is then followed by delayed steps of 30 degrees, 60 degrees, 30 degrees, 60 degrees, 30 degrees, and 30 degrees to illustrate one full cycle of operation at each of the angles in all four quadrants. The specific device carrying the current is noted inside the current waveform. For each one-cycle segment, angle between the phase current and the phase voltage is shown by a phasor diagram just below the one cycle waveform. Number 1 on top and 4 below the square wave is the number of the device turned on during each half-cycle.

Starting from the beginning of the waveform, during the first one-cycle segment of inverter operation with unity power factor, device 1 is turned on with the current flow from the \( +V/2 \) bus into the ac phase for the first full half-cycle. This is followed by turn-off of device 1 and turn-on of device 4, which results in the current flow from the ac phase into the \( -V/2 \) bus via device 4. During this full cycle, the phase-leg works as an inverter with a unity power factor. Note that no diodes are involved in conduction. It is also worth noting that the current transfer is at the natural current zero, i.e., device 1 turns off and device 4 turns on (and vice versa) when the current is zero. With zero-current switching, so-called “soft-switching,” turn-on and turn-off events involve much lower device stresses and switching losses, compared to the switching when current is at its highest operating level.

For the next half-cycle, the turn-off of device 1 and turn-on of device 4 is delayed by 60 degrees in order to change the phase angle for the following one cycle [segment 2 in Figure 3.5(b)] by 60 degrees. It is seen that, as the current polarity reverses, the current transfers from device 1 to diode 1’. For the one-cycle segment 2, the converter operates as an inverter with current lagging the voltage by 120 degrees, i.e., with inductive reactive power. In this one-cycle segment, turn-off device 4 conducts for 120 degrees feeding power from dc to ac (inverter action), and then diode 4’ conducts
Section 3.6 - Sequence of Valve Conduction Process in Each Phase-Leg

- $i_a$ Valve 1 on current in 1
- $-i_a$ Valve 4 on current in 4'
- $+i_a$ Valve 1 on current in 1'
- $+i_a$ Valve 4 on current in 4

Figure 3.5 Operation of a phase-leg through four quadrants: (a) Phase-leg; (b) Waveforms and phasor diagrams through all four quadrants.

for 60 degrees feeding power back from ac to dc (rectifier action). This is then followed by 120 degrees conduction of device 1 feeding power from dc to ac and diode 1' feeding power from ac to dc for the final 60 degrees. Note now that the transfer from turn-off device 4 to turn-off device 1 takes place via diode 4' and from 1 to 4 via diode 1'. Also turn-off of devices 1 and 4 is at natural current zero (soft turn-off). However, turn-on of devices 1 and 4 occurs when current is large and voltage across the valves is $V_d$. This is known as hard turn-on with significant associated device
losses. However, the device capability is often limited by the hard turn-off current requirements so that, notwithstanding the switching losses, the turn-off duty is the most onerous for device capability.

The sequence is repeated by delaying transfer from 4' to 1 by another 30 degrees. Operation in segment 3 now corresponds to current lagging the voltage by 90 degrees, the converter acting as a pure inductor. In this operation, device 1 conducts for 90 degrees feeding power from dc to ac, then current is transferred to diode 1' which conducts for 90 degrees feeding power back from ac to dc. For the next half cycle, current is transferred from diode 1' to device 4 feeding power from dc to ac for 90 degrees, and then from device 4 to diode 4' feeding power back from ac to dc for 90 degrees. Note again that turn-off of devices 1 and 4 occurs at natural current zero when current transfers to diodes 1' and 4', respectively, but the turn-on is hard.

With further delay of 60 degrees, the converter now operates (one-cycle waveform in segment 4) as a rectifier in inductive mode with current lagging voltage by 30 degrees. This is followed by further delay of 30 degrees and one cycle of segment 5 when the converter operates as a rectifier with a unity power factor. Note that in this mode, only the diodes are involved in conduction. Current transfers naturally from 1' to 4' and vice versa during current polarity reversal.

With another delay of 60 degrees, segment 6 shows operation as a rectifier, now in capacitive mode with current leading the voltage by 60 degrees. Note that in capacitive mode, turn-off devices have to turn off high current (transfer from 1 to 4' and 4 to 1') with a corresponding positive voltage jump of \( V_d \). As mentioned earlier for turn-off devices, the maximum current they have to turn off, accompanied by the magnitude of forward voltage jump during turn-off, is the most important limiting parameter of the devices' usable capability, because turn-off is much harsher than turn-on for such devices. In capacitive mode, the turn-on is soft, but the turn-off is hard, which is the reverse of the operation in an inductive mode.

With another delay of 30 degrees, segment 7 shows pure capacitive operation. It is now seen that the sequence of transfer is 1'–1–4'–4–1', each conducting for 90 degrees, 1 and 4 feeding power from dc to ac, and 1' and 4' feeding power from ac to dc. Note that this transfer sequence is the reverse of the sequence for pure inductive mode of 1–1'–4–4'–1 accomplished with 180 degrees phase delay from segment 3. Note also, that in segment 7, the current transfer from 1 to 4' and from 4 to 1' involves turn-off of devices 1 and 4 at maximum current, their most severe duty.

From Figure 3.5, it is seen that for the sequential change of phase angle described above, the conduction and transfer of current takes place as follows:

\[ 1-4-1-1'-4'-1-1'-4'-1-1'-4'-1-1'-4'-1-1'-4'-1-1'-4'-1' \]

\[ 4'-1'-1-4'-1-1'-4'-1-1'-4'-1-1'-4'-1' \]

It should be noted that in inductive operation, all turn-off devices turn off at current zero during current reversal, and therefore turn-offs are soft, i.e., the current is zero when the voltage across the turn-off device rises to \( V_d \). Thus, the turn-off stresses and losses are minimal. Also, in inductive mode, events of the current transfer are from the turn-off device to its own parallel diode, i.e., 1 to 1' or 4 to 4'. In capacitive mode, turn-off is hard, i.e., at finite current, and turn-offs are transfers to the opposite diode, i.e., 1 to 4' or 4 to 1'.

When the transfer is from one turn-off device to another turn-off device, i.e., 1 to 4 or 4 to 1 during inverter operation with unity power factor, it is essential to delay the turn-on for at least several tens of microseconds following the turn-off of the complementary device is complete. This is to ensure that there is no chance of simulta-
neous conduction of devices 1 and 4, which represents a direct short circuit across the dc bus capacitor. It is important to note from the sequence of transfers shown above with reference to Figure 3.5, that except for unity power-factor inverter operation, all the current transfers are from a device to a diode, or from a diode to a device. Thus there is very little risk of shoot-through in a topology that involves one conduction pulse per half-cycle.

Also, since power devices and transformers have losses, these losses have to be supplied from the dc side or the ac side during inverter or rectifier operation respectively. However, during full inductive or capacitive operation, losses can be supplied from either side by operating very slightly in rectifier or inverter mode.

It should now be clear that by having two phase-legs on the same dc bus, with 180 degrees phase shifted in their pulse sequence, would give a single-phase full-wave converter. A total of three such phase legs with a pulse sequence 120 degrees apart would give a three-phase, full-wave converter.

One important point to note is that, in the converter described above, the ac voltage output is strictly a function of dc voltage. For an effective interaction with the ac system, it is often necessary to vary the converter ac output voltage, which means that dc voltage is variable accordingly. This can be done by charging/discharging the dc capacitor from another source/absorber of power or from the ac side of the converter itself. The speed with which the dc voltage can be changed would determine the response time of the converter. For a number of applications, the response time for changing the dc bus voltage would more than adequate. However, in some applications, the dc source assigned to control the dc bus voltage may have other functional priorities. An important point to make here is that an alternate approach is to have a voltage-sourced converter, which has a stiff dc bus, yet be able to vary the ac voltage of the converter. Indeed, there are such converters, the so-called multistep converters and pulse-width modulation converters. These are discussed later in this chapter.

### 3.7 TRANSFORMER CONNECTIONS FOR 12-PULSE OPERATION

In Section 3.5, harmonic content of the phase-to-phase voltage and phase-to-neutral voltage was discussed, and it was mentioned that the two voltages were 30 degrees out of phase. If this phase shift is corrected, then for the phase to neutral voltage, i.e., \( v_{an} \), the harmonics, other than those of the order of 12\( n \) ± 1, would be in phase opposition to those of the phase-to-phase voltage \( v_{ab} \) and with \( 1/\sqrt{3} \) times the amplitude. It follows then, as shown in Figure 3.6(a), that if the phase-to-phase voltages of a second converter were connected to a delta-connected secondary of a second transformer, with \( \sqrt{3} \) times the turns compared to the wye-connected secondary, and the pulse train of one converter was shifted by 30 degrees with respect to the other (in order to bring \( v_{ab} \) and \( v_{an} \) to be in phase), the combined output voltage would have a 12-pulse waveform, with harmonics of the order of 12\( n \) ± 1, i.e., 11th, 13th, 23rd, 25th . . . , and with amplitudes of 1/11th, 1/13th, 1/23rd, 1/25th . . . , respectively, compared to the fundamental. Figure 3.6(b) shows the two waveforms \( v_{an} \) and \( v_{ab} \), adjusted for the transformer ratio and one of them phase displaced by 30 degrees. These two waveforms are then added to give the third waveform, which is seen to be a 12-pulse waveform, closer to being a sine wave than each of the six-pulse waveform.

In the arrangement of Figure 3.6(a), the two six-pulse converters, involving a total of six phase-legs are connected in parallel on the same dc bus, and work together as a 12-pulse converter. It is necessary to have two separate transformers, otherwise
Figure 3.6 Twelve-pulse voltage-sourced converter: (a) 12-pulse converter with wye and delta secondaries; (b) 12-pulse waveform from two six-pulse waveforms; (c) 12-pulse converter with two series connected six-pulse converters.
phase shift in the non-12-pulse harmonics, i.e., 5th, 7th, 17th, 19th ... in the secondaries will result in a large circulating current due to common core flux. To the non-12-pulse voltage harmonics, common core flux will represent a near short circuit. Also for the same reason, the two primary side windings should not be directly connected in parallel to the same three-phase ac busbars on the primary side. Again this is because the non-12-pulse voltage harmonics, i.e., 5th, 7th, 17th, 19th ..., while they cancel out looking into the ac system, would be in phase for the closed loop. Consequently, a large current corresponding to these harmonics will also flow in this loop, limited only by the impedance of the loop, which is essentially the leakage inductance of the transformers.

The circulating current of each non-12-pulse harmonic is given by:

\[ I_n/I_1 = 100/(X_f \ast n^2) \text{ percent} \]

where, \( I_1 \) is the nominal fundamental current, \( n \) is the relevant harmonic number, and \( X_f \) is the per unit transformer impedance of each transformer at the fundamental frequency. For example, if \( X_f \) is 0.15 per unit at fundamental frequency, then the circulating current for the fifth harmonic will be 26.6%, seventh, 14.9%, eleventh, 5.5%, thirteenth, 3.9% of the rated fundamental current, and so on. Clearly this is not acceptable for practical voltage sourced converters. Therefore, it is necessary to connect the transformer primaries of two separate transformers in series, and connect the combination to the ac bus as shown in Figure 3.6(a). With the arrangement shown in Figure 3.6(a), the 5th, 7th, 17th, 19th ... harmonic voltages cancel out, and the two fundamental voltages add up, as shown in Figure 3.6(b), and the combined unit becomes a true 12-pulse converter.

The two converters can also be connected in series on the dc side for a 12-pulse converter of twice the dc voltage, Figure 3.6(c). In such a case, it is important to provide a control to ensure that the two dc buses (capacitors) have equal voltages. The dc voltage of either converter can be increased or decreased by shifting the operation in the rectifier or inverter direction, by a dc voltage balancing control.

There are other means of paralleling voltage source converters on the ac side, which involve transformers with special windings. However, it is generally recognized that special transformers would cost more than the means described above.

Increase in pulse number also decreases the dc side current harmonics, which are cancelled out among the phase legs and do not even enter the dc bus. For 12-pulse converters, the harmonics of the order 6th, 18th, ... are cancelled out, and only the 12-pulse harmonics 12th, 24th ... enter the dc bus.

3.8 24- AND 48-PULSE OPERATION

Two 12-pulse converters, phase shifted by 15 degrees from each other, can provide a 24-pulse converter, obviously with much lower harmonics on ac and dc side. Its ac output voltage would have \( 24n \pm 1 \) order harmonics, i.e., 23rd, 25th, 47th, 49th ... harmonics, with magnitudes of 1/23rd, 1/25th, 1/47th, 1/49th ..., respectively, of the fundamental ac voltage. The question now is how to arrange this 15 degrees phase shift.

One approach is to provide 15 degrees phase-shift windings on the two transformers of one of the two 12-pulse converters. Another approach is to provide phase-shift windings for +7.5 degrees phase shift on the two transformers of one 12-pulse converter and -7.5 degrees on the two transformers of the other 12-pulse converter, as shown in Figure 3.7(a). The latter is preferred because it requires transformers of the same
Figure 3.7 Various means to obtain 24-pulse converter operation: (a) 24-pulse converter transformer connections with two 12-pulse converters in series on the ac side; (b) 24-pulse converter transformer connections with two 12-pulse converters in parallel on the ac side.

design and leakage inductances. It is also necessary to shift the firing pulses of one 12-pulse converter by 15 degrees with respect to the other.

All four six-pulse converters can be connected on the dc side in parallel, i.e., 12 phase-legs in parallel. Alternately all four six-pulse converters can be connected in series for high voltage, or two pair of 12-pulse series converters may then be connected in parallel. Each six-pulse converter will have a separate transformer, two with wye-connected secondaries, and the other two with delta-connected secondaries. Primaries of all four transformers can be connected in series as shown in Figure 3.7(b) in order to avoid harmonic circulation current corresponding the 12-pulse order, i.e., 11th, 13th, 23rd, 24th.

It may be worthwhile to consider two 12-pulse converters connected in parallel on the ac system busbars, with interphase reactors as shown in Figure 3.7(b), for a penalty of small harmonic circulation inside the converter loop. While this may be manageable from the point of view of converter rating, care has to be exercised in the design of the converter controls, particularly during light load when the harmonic currents could become the significant part of the ac current flowing through the converter. An increase in the transformer impedance to, say, 0.2 per unit may be appropriate when connecting two 12-pulse transformers to the ac bus directly and less than that when connected through interphase reactors.

For high-power FACTS Controllers, from the point of view of the ac system, even a 24-pulse converter without ac filters could have voltage harmonics, which are higher than the acceptable level. In this case, a single high-pass filter tuned to the 23rd–25th harmonics located on the system side of the converter transformers should be adequate. The alternative, of course, is go to 48-pulse operation with eight six-pulse groups, with one set of transformers of one 24-pulse converter phase-shifted.
from the other by 7.5 degrees, or one set shifted by +3.75 degrees and the other by -3.75 degrees. Logically, all eight transformer primaries may be connected in series, but because of the small phase shift (i.e., 7.5 degrees), the primaries of the two 24-pulse converters (each with four primaries in series) may be connected in parallel if the consequent circulating current is acceptable. This should not be much of a problem because the higher the order of a harmonic, the lower would be the circulating current. For 0.1 per unit transformer impedance and the 23rd harmonic, the circulating current would be 1.9% only. The circulating current can be further limited by higher transformer inductance or by inter-phase reactors at the point of parallel connection of the two 24-pulse converters. With 48-pulse operation, ac filters should not be necessary.

3.9 THREE-LEVEL VOLTAGE-SOURCED CONVERTER

3.9.1 Operation of Three-Level Converter

It was mentioned earlier in this chapter that it would be desirable to vary the magnitude of ac output voltage without having to change the magnitude of the dc voltage. The three-level converter is one concept that can accomplish that to some extent. One phase-leg of a three-level converter is shown in Figure 3.8(a). The other two phase-legs (not shown) would be connected across the same dc busbars and the clamping diodes connected to the same midpoint \( N \) of the dc capacitor. It is seen that each half of the phase leg is split into two series connected valves, i.e., \( 1-1' \) is split into \( 1 \) and \( 1A-1'A \). The midpoint of the split valves is connected by diodes \( D_t \) to the midpoint \( N \) as shown. On the face of it, this may seem like doubling the number of valves from two to four per phase-leg in addition to providing two extra diode valves. However, doubling the number of valves with the same voltage

![Figure 3.8 Operation of a three-level converter: (a) One phase-leg of a three-level converter; (b) Output ac voltage.](image-url)
rating would double the dc voltage and hence the power capacity of the converter. Thus only the addition of the diode clamping valves, $D_1$ and $D_2$, per phase-leg, Figure 3.8(a), adds to the converter cost. If the converter is a high-voltage converter with devices in series, then the number of main devices would be about the same. A diode clamp at the midpoint may also help ensure a more decisive voltage sharing between the two valve-halves. On the other hand, requirement that a converer continue safe operation with one failed device in a string of series connected devices, may require some extra devices.

Figure 3.8(b) shows output voltage corresponding to one three-level phase leg. The first waveform shown is a full 180 degrees square wave obtained by the closing of devices 1 and 1A to give $+V_d/2$ for 180 degrees, and the closing of valves 4 and 4A for 180 degrees to give $-V_d/2$ for 180 degrees. Now consider the second voltage waveform in Figure 3.8(b) in which the upper device 1 is turned off and device 4A is turned on an angle $\alpha$ earlier than they were due in the 180 degrees square wave operation. This leaves only device 1A and 4A on, which in combination with diodes $D_1$ and $D_2$, clamp the phase voltage $V_a$ to zero with respect to the dc midpoint $N$ regardless of which way the current is flowing. This continues for a period $2\alpha$ until device 1A is turned off, and device 4 is turned on, and the voltage jumps to $-V_d/2$ with both the lower devices 4 and 4A turned on and both the upper devices 1 and 1A turned off, and so on. Of course, angle $\alpha$ is variable, and the output voltage $V_a$ is made up of $\sigma = 180^\circ - 2\alpha^\circ$, square waves. This variable period $\sigma$ per half-cycle, potentially allows the voltage $V_a$ to be independently variable with potentially a fast response. It is seen that devices 1A and 4A are turned on for 180 degrees during each cycle, devices 1 and 4 are turned on for $\sigma = 180^\circ - 2\alpha^\circ$ during each cycle, while diodes $D_1$ and $D_4$ conduct for $2\alpha^\circ = 180^\circ\sigma$ each cycle. The converter is referred to as three-level because the dc voltage has three levels, i.e., $-V_d/2$, 0, and $+V_d/2$.

As explained earlier, these phase-legs can handle the current flow in any phase relationship. Turn-off devices handle any instantaneous inverter action and their parallel diodes handle any instantaneous rectifier action. Clamping diodes $D_1$ or $D_4$, along with lower devices 1A and 4A, carry the current during clamping periods, with $D_1$-1A carrying the negative current (current going into the ac bus) and $D_4$-4A carrying the positive current.

Also as explained before for the two-level phase-legs, these three-level phase-legs can also be connected in different configurations to obtain the required converter. These configurations include a single phase, full-wave converter with two legs, a three-phase bridge converter with three legs and wye-connected secondaries with floating neutral or delta-connected secondaries, etc. Figure 3.7(b) also shows the output voltage of the second phase $v_b$ and the phase-to-phase voltage $v_{ab}$ for a three-phase converter. As discussed previously, the triplen harmonics will not pass through to the primaries with floating neutral, etc. Two six-pulse converters can provide a 12-pulse converter, and so on.

With the three-level converter it should be noted that for the duration of zero output voltage, Figure 3.8(b), the phase-leg current(s) flows into the midpoint of the two capacitors and thus flows through the dc capacitor. This current is mainly of third harmonic and is substantially independent of the converter pulse number.

### 3.9.2 Fundamental and Harmonic Voltages for a Three-Level Converter

What the three-level converter buys is the flexibility to rapidly vary the ac voltage or to provide a defined zero voltage “notch” to eliminate or reduce some specific harmonics. However, when considering the harmonics, there is a limitation in exploitation of this flexibility, as explained in the following paragraphs.
Taking into account the ac voltage pulse width of duration \( \sigma \) per half-cycle, the magnitudes of fundamental and harmonic components of phase-to-dc-neutral voltage are defined by

\[
v = \frac{4}{\pi} \left( \frac{V_d}{2} \right) \sin \left( \frac{\sigma}{2} \sin \left( \omega t + \frac{\sigma}{2} \right) - \frac{1}{3} \sin \left( \frac{3\sigma}{2} \sin \left( \omega t + \frac{\sigma}{2} \right) + \frac{1}{5} \ldots \right) \]
\]

which gives

\[
v_n = \frac{4}{\pi} \left( \frac{V_d}{2} \right) \left[ \frac{1}{n} \sin \frac{n\sigma}{2} \sin \left( \omega t + \frac{\sigma}{2} \right) \right]
\]

RMS value is given by

\[
V_n = \frac{2\sqrt{2}}{\pi} \left( \frac{V_d}{2} \right) \frac{1}{2} \sin \frac{n\sigma}{2}
\]

Fundamental rms voltage is given by

\[
V_1 = \frac{2\sqrt{2}}{\pi} \left( \frac{V_d}{2} \right) \sin \frac{\sigma}{2}
\]

which starts from a maximum rms value of \((\sqrt{2}/\pi) V_d\) at \( \sigma = 180^\circ \), and reaches zero at \( \sigma = 0^\circ \).

If \( V_1 \) is assumed to be \( V_{1\text{max}} = (\sqrt{2}/\pi) V_d = 1 \text{ pu} \) at \( \sigma = 180^\circ \), Figure 3.9 shows the value of the fundamental voltage \( V_1 \) as per unit of \( V_{1\text{max}} \) and function of the pulse width, \( \sigma \). As seen, the fundamental is 1.0 p.u. at \( \sigma = 180^\circ \), and decreases with decreasing pulse width, decreasing to zero at \( \sigma = 0^\circ \).

Figure 3.9 also shows the values of harmonics, as per unit of the actual fundamental voltage \( V_1 \), as a function of the pulse width \( \sigma \). Harmonic values as per unit of \( V_{1\text{max}} \) can be more useful, if the purpose is to consider harmonics in terms of the specified distortion levels. Such values can be obtained by multiplying a harmonic level in Figure 3.9 by corresponding per unit fundamental level.

It is interesting to note the variation in per unit harmonics with decrease in \( \sigma \) (increase in \( 2\alpha = 180^\circ - \sigma \)). It is seen that the 5th, 7th \ldots harmonics are at their maximum, 0.2 p.u. and 0.143 p.u., respectively, at \( \sigma = 180^\circ \), and then decrease and increase according to the equation above. A particular harmonic reaches zero, when

\[180^\circ - \sigma = (180^\circ/n), \text{ where } n \text{ is the harmonic number.}\]

For fifth harmonics, this occurs at \( \sigma = 144^\circ \) and again at \( 72^\circ \).

The seventh harmonic is zero when \( \sigma = 154.3^\circ, 102.9^\circ, \text{ and } 77^\circ \).

After the first zero, each harmonic rises again, reaching a peak at

\[180^\circ - \sigma = 2\pi(180^\circ/n).\]

These peaks are higher than the first peaks because the values shown are per unit of the actual declining magnitude of the fundamental voltage \( V_1 \). All harmonics eventually approach 1.0 p.u. at \( \sigma = 0^\circ \) when the fundamental approaches zero.

It is noted that for operation with \( \sigma \) within 154 degrees to 144 degrees, both the fifth and seventh harmonics are very low, and the converter almost behaves like a 12-pulse converter. For operation at \( \sigma = 144^\circ \), the fundamental voltage also drops to 0.95 p.u., which in effect represents 5% loss of capacity.

As an alternative, it may be preferred to normally operate a three-level converter.
at about 154 degrees, which is where the fourth harmonic is zero, and the fifth harmonic is about half of its maximum value. In any case, it is a matter of compromising flexibility of voltage control, reduction of specific harmonics, and some loss of useable capacity. In many applications, it is not necessary to vary the ac voltage independently of the dc voltage, in which case a three-level converter would be a good way to reduce low order harmonics or to eliminate a specific harmonic. Alternately, one can normally operate the three-level converter with varying $\sigma$ over a range from $\sigma = 180^\circ$ down to $\sigma = 90^\circ$, giving a variable ac voltage from 100% to 70%. It also points to the consideration of a combination of higher pulse converter, dc bus voltage control and use of three-level phase-legs. Unless the three-step converter is used within a multipulse structure, it is useful for only a limited range of independent ac voltage control. This is because the percentage harmonics increase rapidly with decrease in the fundamental output voltage to below about 70%, as shown by Figure 3.9.

With the split dc capacitor level, it is essential to ensure that the two capacitors are charged to equal voltage because unequal voltages will generate even harmonics. Capacitor voltage balance is achieved by a control, which prolongs or shortens the conduction time of the appropriate devices.

These curves of Figure 3.9 also apply to any other configuration that is based on square wave with pulse width less than 180 degrees. Note that all the triple harmonics are zero at $\sigma = 60^\circ$, which corresponds to the phase-phase six-pulse voltage waveform for a three-phase full wave bridge (discussed in Section 3.5).
A significant disadvantage of a three-level converter is that with increasing \( \sigma \), an increasing amount of third harmonic flows into the midpoint of the dc capacitor. This current generates a third harmonic voltage across the capacitors. In order to keep this harmonic voltage within acceptable limits (to avoid generation of additional harmonics in the ac output and an increase in the converter current rating), the size of the dc capacitor has to be increased compared to that of the two-level converter.

### 3.9.3 Three-Level Converter with Parallel Legs

There is yet another method of achieving a three-level converter, which is to connect two phase-legs in parallel per phase as shown in Figure 3.10(a). The two legs are paralleled through an inductor and the ac connection is made at the midpoint of this inductor, and their pulse sets are phase shifted by an angle \( \alpha \) each in the opposite directions (a total of \( 2\alpha \)). The ac terminal voltage of the two phase-legs, with respect to a hypothetical dc midpoint, are shown in Figure 3.10(b) by the first two waveforms, shifted from each other by an angle, \( 2\alpha \). The net ac terminal voltage, with respect to the dc midpoint, is the average of the two voltages, and is shown by the third waveform. It consists of a half-cycle pulse of variable duration \( \sigma = 180 - 2\alpha^2 \), the same as for the three-level converter with split capacitor discussed above. The harmonic content is the same as shown by Figure 3.9. The inductor voltage is given by the difference of the ac voltage of the two legs, and is shown by the fourth waveform of Figure 3.10(b), which conveys that greater the required range of control, larger would be the inductor size. Its MVA rating would be directly proportional to the integral of the voltage \( V_L \).

It is natural to suppose that one can go to higher levels, i.e., four-level, five-level, and so on. However, detailed consideration of these higher level topologies would reveal a major problem of voltage balancing between the capacitors. It is not reasonable to assume that the current flow though each level is balanced within some tolerable range for a converter to continue to operate in five-level mode on its own. However, if there is a two-converter system, with dc bus in between, it is possible to link the two converters in a way to ensure balanced capacitor voltages of different levels.

### 3.10 PULSE-WIDTH MODULATION (PWM) CONVERTER

In two-level or multilevel converters, there is only one turn-on, turn-off per device per cycle. With these converters, the ac output voltage can be controlled, by varying the width of the voltage pulses, and/or the amplitude of the dc bus voltage. Another approach is to have multiple pulses per half-cycle, and then vary the width of the pulses to vary the amplitude of the ac voltage. The principal reason for doing so is to be able to vary the ac output voltage and to reduce the low-order harmonics, as will be explained here briefly. It goes without saying that more pulses means more switching losses, so that the gains from the use of PWM have to be sufficient to justify an increase in switching losses. There are also resonant PWM converter topologies that incorporate current-zero or voltage-zero type soft switching, in order to reduce the switching losses. Such converters are being increasingly utilized in some low power applications, but with the known topologies, they have not been justifiable at high power levels due to higher equipment cost.
Chapter 3 ■ Voltage-Sourced Converters

Figure 3.10 Operation of three-level converter with parallel legs: (a) One phase-leg with two parallel legs; (b) Waveforms for the two parallel legs.

PWM converters of low voltage and low power in the range of tens of watts, for, say, printed circuit boards’ power supplies, may have internal PWM frequency in the hundreds of kilohertz. Industrial drives in tens of kilowatts may have internal PWM frequency in the tens of kilohertz. For converters in the 1 MW range, such as for Custom Power, the frequency may be in a few kilohertz range. For FACTS technology with high power in the tens of megawatts and converter voltage in kVs and tens of kVs, low frequencies in the few hundred Hertz or maybe the low kilohertz range may seem feasible and worth considering.

Consider again a phase-leg, shown in Figure 3.11(a) [which is the same as Figure 3.5(a)], as part of a three-phase bridge converter. Figure 3.10(b) shows comparison of two types of control signals, three signals of main-frequency sine wave representing three phases, and a sawtooth wave signal of nine times the main frequency (540 Hz
Section 3.10 ■ Pulse-Width Modulation (PWM) Converter

Figure 3.11 Operation of a PWM converter with switching frequency of nine times the fundamental: (a) A phase-leg; (b) PWM waveforms.

for 60 Hz main frequency). Turn-on and turn-off pulses to the devices correspond to the crossing points of the sawtooth wave with the sine wave of corresponding phase. The negative slope of the sawtooth wave crossing the sine wave of phase a, results in a turn-on pulse for device 1 and turn-off pulse for device 4. The positive slope of the sawtooth wave crossing the sine wave of phase a results in a turn-off pulse for device 1 and turn-on pulse for device 4. The resulting voltage of the ac terminal a, with respect to hypothetical midpoint N of the dc capacitor, is shown in hatch in Figure 3.11(b). In comparison to Figure 3.5(b) with two square pulses per cycle, the waveform of Figure 3.11(b) is made up of nine square pulse cycles of varying width per main frequency cycle. The pulses are wider in the middle of each half sine wave compared to the ends of the half sine wave.

The following observations are worth noting with respect to the waveforms of Figure 3.11(b):

1. The output voltage waveform contains a fundamental frequency component and harmonics.
2. The output voltage pulses are symmetrical about the zero crossings of the sine wave, because the sawtooth frequency is an odd integer multiple of the main frequency. Any even multiple will create asymmetry about the zero crossing, which will contain even harmonics. Non-integer multiples are even worse as they create sub- and supersynchronous harmonics as well. When the frequency is high, above a few kilohertz, this asymmetry becomes insignificant, but at the low PWM frequencies synchronization of the control signals is important.

3. With a fixed sawtooth wave, increasing the magnitude of the sine wave will increase the conduction time of device 1, and decrease the conduction time of device 4 for the positive half-cycle and vice versa for the negative half-cycle. This means that the fundamental component of the ac voltage \( V_{an} \) and hence the output ac voltage will increase with an increase in the magnitude of the control sine wave and decrease with a decrease in the magnitude of the control sine wave. For control sine wave peak less than the sawtooth-wave peak, the output ac voltage varies linearly with variation of the control sine wave.

4. As the control sine-wave peak equals the peak of the sawtooth wave, the middle notch in the ac output voltage disappears. If the control sine wave is increased to a higher and higher magnitude, more and more notches will disappear and the output voltage will eventually become a single square wave per half-cycle.

5. It is clear that the ac output voltage can be controlled from zero to maximum.

6. The sine wave itself can be modified with notches, etc. to create other effects on the waveform.

The order of harmonics present in this type of PWM waveform is determined by \( k_1n \pm k_2 \), where \( k_1 \) is the frequency multiplier (9 for Figure 3.11) of the carrier frequency, and \( n \) and \( k_2 \) are integers. However, \( k_2 \) may only be taken up to 2, after which the magnitude of that harmonic order becomes rather small. Due to half-cycle symmetry, all the even order harmonics also disappear. Furthermore in a three-phase bridge circuit, all of the triple harmonics, i.e., 3rd, 9th, . . . , are eliminated. Also, if the carrier frequency is a multiple of 3, even the harmonics of the order of the carrier frequency are cancelled out in the phase-to-phase and phase to the floating-neutral voltages.

Thus, for the chosen frequency multiplier 9, the order of harmonics is given as: 5th, 7th, 11th, 13th . . . (all the harmonics except the even and triple harmonics), as for the six-pulse three-step converter discussed in Section 3.9. However, in the PWM case shown the fifth harmonic will be very small.

Figure 3.12 shows PWM output voltage waveforms corresponding to a PWM frequency of three times the main frequency. The first waveform shows the control signals, similar to those in Figure 3.11. Second waveform is the phase a to dc neutral voltage \( V_{an} \). It is seen that it has one notch in the center of each half-cycle and the width of this notch is dynamically controllable every half-cycle. The third waveform is \( V_{bn} \), the output voltage of phase b to dc neutral voltage, which obviously is the same as \( V_{an} \) except the phase delay of 120 degrees. Subtracting \( V_{bn} \) from \( V_{an} \) gives the phase–phase voltage \( V_{ab} \), as shown by the fourth waveform. This shows two notches resulting from the crossings of the control signals. The next waveform is that of the \( V_{an} \), the voltage between the floating neutral \( n \) of a wye-connected floating secondary and the dc neutral. This is obtained by adding and averaging the three ac voltages.
\( u_{aN}, u_{bN}, \) and \( u_{cN} \) (\( u_{iN} \) not shown). Subtracting \( u_{iN} \) from \( u_{aN} \) gives the last waveform shown in Figure 3.12, that of the transformer phase-to-neutral voltage. Because of the half-wave symmetry, all the ac waveforms are free from even harmonics. Waveforms \( u_{ab} \) and \( u_{an} \) are free from triplen harmonics and the \( u_{an} \) lags \( u_{ab} \) by 30 degrees. As explained earlier in Section 3.7, combining these two waveforms through separate wye and delta transformers, will result in a 12-pulse converter, which will have adequate flexibility of rapid ac voltage control without having to change the dc voltage level. The control of the dc voltage can then be optimized for other considerations.

It should now be obvious that the ac voltage waveform can be chopped in many different ways with different control waveforms and numerical program. There are a variety of waveforms other than sinusoidal and sawtooth that are used to create ac output voltage with fewer low-frequency harmonics and fewest notches.

While chopping of the waveforms and showing PWM waveforms is easy on paper, it is not a trivial matter when we consider its implications for design of high-power and high-voltage converters. In terms of switching losses, impact of increased higher harmonics, EMI, audible noise, etc. has to be justified by appropriate gains in other areas, particularly if it helps satisfy the harmonic requirements without having to go to a pulse number higher than 12 for modest size converters. Nevertheless, a considered use of PWM or notches at low-frequency level has its merits, particularly for the FACTS Controllers of lower power levels of, say, 10–50 MW, as will be seen from the next section.

### 3.11 GENERALIZED TECHNIQUE OF HARMONIC ELIMINATION AND VOLTAGE CONTROL

One effective way to have the freedom of controlling the voltage and also eliminating lower order harmonics is a method pioneered by Patel and Hoft in the early 1970s. It involves varying specific notches (also referred to as chops) in the square wave such that specific harmonics are eliminated from the waveform. This is explained below.

Basically, a square wave can be chopped a number of times in a relationship that eliminates a number of harmonics, as well as giving flexibility to vary the fundamental voltage. With \( M \) number of chops, there are \( M \) degrees of freedom. One of these degrees of freedom can be used to control the fundamental leaving the other \( M-1 \) degrees of freedom used to eliminate \( M-1 \) selected harmonics.

It is seen from Figure 3.11(b), that a sawtooth wave with nine times fundamental frequency has four notches each in the positive and negative half-cycle waveform. They also have half-wave and quarter-wave symmetry. It follows that with proper firing angles as well as half-wave/quarter-wave symmetry, not only the fundamental frequency component can be controlled, but the three other selected harmonics can be eliminated, i.e., 5th, 7th, and 11th, from the output ac voltage of a three-phase full wave bridge. If there were two three-phase bridges, phase-shifted as previously discussed in this chapter, forming a 12-pulse voltage sourced converter, then the harmonics that would need eliminating would be the three lowest, i.e., 11th, 13th, and 23rd. With a limited number of notches, it is possible to almost achieve the equivalent of 24-pulse operation with two three-phase six-pulse converters. On the other hand, it must be mentioned that with PWM operation, the higher harmonics will have relatively higher magnitudes than with the single-pulse operation, although higher harmonics are easier to filter out. If the low-order harmonics are eliminated, then with a high-pass filter for higher harmonics, a near sinusoidal current flow can be obtained.
Figure 3.12 Operation of a PWM converter with switching frequency of three times the fundamental frequency.
With three notches per half-cycle, one can eliminate the fifth and seventh harmonics from a six-pulse converter, or eliminate the eleventh and thirteenth from a 12-pulse converter, and so on.

Figure 3.11(b) conveys a generalized half-wave output waveform with $M$ notches defined by angles $\alpha_0$, $\alpha_1$, $\alpha_2$, \ldots $\alpha_{2M-1}$, with angles $\alpha_1$ and $\alpha_2$ defining the first notch. With $2M = 9$, in the example of Figure 3.11, $M = 4$ representing four notches per half-cycle. The generalized waveform of ac voltage $v_{an}$ for a phase leg has a voltage amplitude of $+V_d/2$ and $-V_d/2$ with respect to the dc midpoint.

Assuming $V_d/2 = 1$ per unit for generalization, and half-wave/quarter-wave symmetry as in the ac voltage waveforms of Figure 3.11, the waveform can be represented by a Fourier series as

$$f(wt) = \sum_{n=1}^{\infty} \left[ a_n \sin(n\omega t) + b_n \cos(n\omega t) \right]$$

where, with half-wave and quarter-wave symmetry, $b_n = 0$, and:

$$a_n = \frac{4}{n\pi} \left[ 1 + 2 \sum_{k=1}^{M} (-1)^k \cos n\omega_k \right]$$

$M-1$ equations can be assigned for the specific targeted harmonics to be eliminated as $a_n = 0$ for these harmonics. The remaining one equation is used for a specific required value of the fundamental voltage with $a_1 = a$, a finite per unit value. By solving these equations, one can obtain specific values of angles $\alpha$ for a specific value of the fundamental voltage.

Thus for four notches per half-cycle, as for Figure 3.11, there will be four equations to be solved to calculate all values of $\alpha$ for turn-on and turn-off pulses corresponding to each discrete value of the fundamental voltage. These are nonlinear equations, and would require large amounts of real time iterative computation and there may be more than one solution for some values. Thus it is preferred to use lookup tables for, say, each 0.5% change in the magnitude of the required ac voltage. The required shift in angles for the required ac voltage variations per step is quite small, and the number of steps can be reduced and the change from step to step linearized.

Clearly with digital controls, this method is superior to the sawtooth sine wave control or any other wave comparison method. The ac fundamental output voltage can be controlled over a wide range, down to perhaps about 10%, without excessive distortion of the current flow or need for a large harmonic filter.

### 3.12 CONVERTER RATING—GENERAL COMMENTS

Assuming that the required converter rating is rather low, the least cost and simplest controllable three-phase converter would seem to be a six-valve converter with one turn-off device/diode per valve. In FACTS applications, there will usually be a need for a transformer between the converter valves and the ac system; there is therefore a certain flexibility provided by the transformer turn ratio to match the available device current and voltage ratings. A six-pulse converter based on one device per valve could yield a maximum rating of, say, 5 MVA. However, even at this low rating, a simple six-pulse converter is unlikely to be the best choice for connection to the ac system on account of harmonic distortion requirements. Complex decisions have to be made on the use of large filters versus higher pulse-order and PWM or quasi-PWM converter topologies, etc., apart from the flexibility required for the control.
One area of needed attention for single-device per valve converters is the consequence of failure of a device. Use of fuses would not be desirable. However given the advances in sensing and digital protection technology, it is not unreasonable to sense a fault event, including a shoot-through in a few microseconds, and turn-off other associated converter valves for an effective safe protection strategy.

Most FACTS applications will involve converters with a rating much higher than 5 MVA. The designer now has many options to meet the needs of the higher rating. These options include:

1. Increase pulse-order to 12, 24, or 48, in order to reduce the harmonics to an acceptable level with 2, 4, or 8 six-pulse converters, duly phase-shifted, one can concurrently increase the total converter rating to a maximum of 10, 20, or 40 MVA, still with one turn-off device per valve. Here, one is faced with the choice of series or parallel connections on the dc side, types of transformer arrangements and phase shift among converters, and series/parallel connections on the ac side. These approaches have to be balanced with the other means of reducing harmonics and acquiring flexibility of dynamic and steady state controls, including three-level, PWM, special notches and combination of the above.

2. Adapting a three-level converter topology also doubles the converter voltage and hence the potential maximum single-device per valve converter capacity to, say, 10 MVA per six-pulse, 20 MVA per 12-pulse, and so on. The three-level topology provides the flexibility of a limited range of independent ac voltage control. But again, this has to be balanced against the low frequency PWM or notch-based topologies to achieve independent ac voltage control. Thus it is seen that a modest size FACTS converter rating can be achieved without having devices in series.

3. Connecting devices in series is the most frequently used option for high-power converters. Here the issue is that of ensuring equal voltage distribution among the devices. While the series connection technique is well known, voltage dividers/snubbers have to be provided and some allowance has to be made in the device voltage rating. It is also a practice to include one extra device/diode in series in each valve to ensure continued operation in the event of failure of a device. Note that when a power semiconductor device fails, it must fail into a short circuit and continue to carry current indefinitely without adverse consequences, other than the fact that failure of a second device/diode in the same valve could lead to a catastrophic failure.

4. Double the number of phase-legs and connect them in parallel; this is shown in Figure 3.10, in which the two phase-legs are connected in parallel via a center-tapped inductor. These phase-legs may be of the two-level or three-level variety.

5. Connect converter groups in parallel. In fact a large number of groups can be connected in parallel beyond what may be needed for increasing the pulse number. With parallel connection of converters, it is necessary to have a protection strategy that isolates a faulty converter, with minimal impact on the operation of the other converters. A 48-pulse converter with all six-pulse converters connected on the same dc bus involves 24 phase legs in parallel. With high-speed sensing and fast turn-off capability of devices, parallel connection of a large number of phase legs is quite feasible. However, considerations
of fault currents, high-current bus work would often lead to a combination of series and parallel connections.

6. Use a combination of two or more of the options mentioned above or any other option not mentioned above, in order to arrive at a converter of required rating and performance. Also given the high relative cost of high-voltage isolation with transformers, there is a strong incentive to somehow come up with a platform-based design, and even a transformer-less design, particularly when a small converter is needed in a high-power transmission.

It is obvious that a designer (supplier) has a large number of options to sort out. If two design teams worked separately, the odds are very much in favor of them arriving at different solutions. It is therefore important that the purchaser of FACTS technology pay more attention to the performance specifications rather than to details of the technical design.

REFERENCES


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References


4.1 BASIC CONCEPT OF CURRENT-SOURCED CONVERTERS

A current-sourced converter is characterized by the fact that the dc current flow is always in one direction and the power flow reverses with the reversal of dc voltage. In this respect, it differs from the voltage-sourced converter in which the dc voltage always has one polarity and the power reversal takes place with reversal of dc current. Figure 4.1 conveys this difference between the current sourced and the voltage-sourced converters.

In Figure 4.1(a), the converter box for the voltage-sourced converter is symbolically shown with a turn-off device with a reverse diode, whereas the converter box for the current-sourced converter, Figure 4.1(b), is shown without a specific type of device. This is because the voltage-sourced converter requires turn-off devices with reverse diodes; the current-sourced converter may be based on diodes, conventional thyristors or the turn-off devices.

Thus there are three principal types of current-sourced converters (Figure 4.2):

1. Diode converter [Figure 4.2(a)], which simply converts ac voltage to dc voltage, and utilizes ac system voltage for commutation of dc current from one valve to another. Obviously the diode-based, line-commutating converter just converts ac power to dc power without any control and also in doing so consumes some reactive power on the ac side.

2. Line-commutated converter, based on conventional thyristors (with gate turn-on but without gate turn-off capability), Figure 4.2(b), utilizes ac system voltage for commutation of current from one valve to another. This converter can convert and control active power in either direction, but in doing so consumes reactive power on the ac side. It can not supply reactive power to the ac system.

3. Self-commutated converter which is based on turn-off devices (GTOs, MTOs, IGCTs, IGBTs, etc.), in which commutation of current from valve to valve takes place with the device turn-off action and provision of ac capacitors, to facilitate transfer of current from valve to valve. Whereas, in a voltage-sourced converter the commutation of current is supported by a stiff dc bus with a dc
Figure 4.1 Voltage-sourced and current-sourced converter concepts: (a) voltage-sourced converter; (b) current-sourced converter.

Figure 4.2 Types of current-sourced converters: (a) diode rectifier; (b) thyristor line-commutated converter; (c) self-commutated converters.
In a self-commutated current-sourced converter, the ac capacitors provide a stiff ac bus for supplying the fast changing current pulses needed for the commutations. Apart from its capability of controlled power flow in either direction, this converter, like the voltage-sourced converter, can also supply or consume controlled reactive power. However, it is interesting to note that even though the converter can supply reactive power, sources of reactive power, i.e., capacitors and ac filters, are needed in any case. An advantage of the converters with turn-off devices (self-commutating converters) is that they offer greater flexibility including PWM mode of operation.

It must be mentioned that when the converters are based on turn-off devices, the voltage-sourced converters have been preferred over the current-sourced converters. In fact, none of the converter-based Controllers described in this book are based on current-sourced converters. However, with evolution in the device characteristics and functional details of the converters, this situation can change in the future. Therefore the current-sourced converters with turn-off devices are not discussed in much detail.

When reactive power management is not a problem, i.e., where controlled reactive power supply is not required and the reactive power consumed by the converters can be supplied from the system capacitors and/or filters, the line-commutated converters have a decisive economic advantage over self-commutated converters. For conversion of ac to dc and dc to ac, in HVDC transmission, line-commutated converters have been used almost exclusively where reactive power is managed through switched capacitors, filters and the power system. The converters for the superconducting storage can well be current-sourced converters since the superconducting reactor is itself a current source. Also the dc power supply for storage means, to drive voltage-sourced converter-based phase-angle regulators, discussed in Chapter 6, can be current-sourced converters. The economic advantage of conventional thyristor based converters arises from the fact that on a per device basis thyristors can handle two to three times the power than the next most powerful devices such as GTOs, IGCTs, MTOs, etc. In any case, an engineer should be familiar with a wide variety of converters and keep an open mind and continuously re-evaluate the converter topologies with the evolution of the power devices and other components of the system.

There are variations of the above basic types of current-sourced converters, including thyristor converters with artificial commutation, resonant converters, and hybrid converters, but they are not discussed in this book.

Since the dc voltage in a current-sourced converter can be in either direction, the converter valves must have both forward and reverse blocking capability. The conventional thyristors are usually made as symmetric devices, i.e., they have both the forward and reverse blocking capability. This is because they are easier and cheaper to make and can be made with peak blocking voltage as high as 12 kV along with a high current carrying capability. On the other hand the turn-off devices have a high on-state forward voltage drop when they are made as symmetric devices. Given the high production volumes of asymmetric turn-off devices, dictated by the industrial market, it may be advantageous to connect an asymmetric turn-off device and a diode in series to get a symmetric device combination. This again results in higher forward voltage drop and losses. Given this and other aspects, such as fast-switching characteris-
tics of IGBTs, the industrial converter market has shifted very much towards the PWM voltage-sourced converters, discussed in Chapter 3.

### 4.2 THREE-PHASE FULL-WAVE DIODE RECTIFIER

Three-phase, full-wave diode rectifier is discussed in some more detail than necessary, in order to build the explanations up to the fully controlled converter. In any case the diode rectifier is very useful as a low-cost source of dc power obtained from an available ac source. Rectifiers with a rating greater than a few tens of KWs will almost always be a three-phase, full-wave circuit, shown in Figure 4.3(a), or a combination of several such circuits.

In order to first simplify the explanation and still be realistic, it is assumed that the dc side inductance is very large and therefore the dc current is constant. The circuit consists of six valves, numbered 1 to 6, the number sequence conveying the order of the current transfer and the dc output voltage. The current commutates from valve to valve to turn it into an ac current.

Figure 4.3(b) shows the three-phase ac waveforms \(v_a, v_b,\) and \(v_c\) with respect to the transformer neutral \(N.\) Assuming that the ac system impedance is zero and the transformer is ideal, the top waveforms of Figure 4.3(b) also show voltage waveforms of the two dc buses, with respect to the transformer neutral. This is followed by the waveforms for the constant dc current, ac current waveforms in relation to constant dc current, and the dc output voltage between the two dc buses.

The beginning of Figure 4.3(b) shows that from instant \(t_1\) to \(t_2,\) valves 1 and 2 are conducting, the dc current takes the path valve 2, into phase c, out of phase a, and valve 1. The dc buses are connected to phases a and c, and the dc output voltage is that between phases a and c, as shown by the thick lines. At point \(t_1\) the voltage of phase b becomes positive with respect to phase a, and valve 3 becomes forward biased. Being a diode, it starts conducting and takes the current over from valve 1 and the output dc voltage follows the voltage between the thick lines of phases b and c. The current waveforms show that the current is flowing through valve 2, phase c, phase b and valve 3. Next at instant \(t_4,\) phase a becomes negative with respect to phase c, and valve 4 becomes forward biased, starts conducting and takes the current over from valve 2. Then at instant \(t_5,\) valve 5 takes over from valve 3, at instant \(t_6\) valve 6 takes over from valve 4, and at instant \(t_1\) valve 1 takes over from valve 5 for one complete cycle. The current in the three phases is shown and is made up of 120 degree blocks of dc current, through an upper and a lower valve of each phase leg.

It should be noted that in a current-sourced converter, the commutation takes place from valve to valve among valves connected to the same dc bus, i.e., valves 1 to 3 to 5 to 1 and so on. This is different from the voltage-sourced converters in which the commutation occurs between the valves connected to the same phase leg, i.e., valve 1 to 4 to 1 and so on. As a result the waveforms of the ac voltage of a voltage-sourced converter are made up of 180 degree blocks and consequently have triplen harmonics; the waveforms of ac current of a three-phase current-sourced converter are made up of 120 degree blocks and consequently do not have triplen harmonics.

The dc output voltage as shown at the top of Figure 4.3(b), is for the two dc buses with respect to the transformer neutral. Adding the magnitude of these two waveforms gives the voltage of the upper dc bus with respect to the lower dc bus. As shown at the bottom of Figure 4.3(b), the dc output voltage has a six-pulse waveform, made up of the sum of two three-phase, half-wave circuits.
Section 4.2 ■ Three-Phase Full-Wave Diode Rectifier

Three-Phase Full-Wave Diode Rectifier

(a) Three-phase, full-wave diode converter neglecting commutation angle:
(a) three-phase full wave six-pulse diode converter; (b) current and voltage waveforms for a three-phase, full-wave diode converter.

Figure 4.3 Three-phase, full-wave diode converter neglecting commutation angle:
(a) three-phase full wave six-pulse diode converter; (b) current and voltage waveforms for a three-phase, full-wave diode converter.
The dc output voltage is made up of 60 degree segments and with the peak of ac voltage as a reference point, it is defined by

\[ e = \sqrt{2} E \cos \omega t \]

where \( E \) is the phase-to-phase voltage. This ideal output voltage is given by

\[ V_o = \frac{3}{\pi} \int_{-\pi/6}^{\pi/6} \sqrt{2} E \cos \omega t \, d(\omega t) \]

\[ = \frac{3\sqrt{2}}{\pi} E [\sin(\omega t)]_{-\pi/6}^{\pi/6} = \frac{3\sqrt{2}}{\pi} E = 1.35 E \]

The output voltage is positive with dc current flowing out of the anode bus of the converter; hence the power flow is from ac to dc (rectifier). DC output voltage contains some harmonics (discussed at the end of Section 4.3). The ac current, Figure 4.3(b), is made up of square wave blocks of 120 degree duration each half-cycle. The rms value of this phase current is given by

\[ I = \frac{\sqrt{2}}{\pi} \int_{-\pi/6}^{\pi/6} I_a^2 \, d(\omega t) \]

\[ = \frac{I_a^2}{\pi} [\sin(\omega t)]_{-\pi/6}^{\pi/6} = \frac{\sqrt{2}}{\sqrt{3}} I_a = 0.816 I_d \]

AC current also has harmonics (further discussed in Section 4.3).

Equating the fundamental ac power and the dc power (neglecting losses),

\[ \sqrt{3} EI = V_d I_d \]

and substituting \( V_d \) in terms of \( E \) from (4.1) gives the rms fundamental ac current:

\[ I_1 = \frac{\sqrt{6}}{\pi} I_d = 0.78 I_d \]

The rms difference between the total rms current \( I \) (4.2), and the rms fundamental current \( I_1 \), is the total rms harmonic current:

\[ I_h = \sqrt{(I^2 - I_1^2)} = 0.24 I_d \]

There was one simplifying assumption in the above discussion that the current instantaneously commutated from valve 1 to 3, 2 to 4, etc. In reality it will take a significant time. Typically it may take about 20 degrees to 30 degrees. The commutation of in-line commutated converters involves transfer of current from one phase to another through the valves in an inductive circuit of the ac system, including the transformer inductance.

Consider again the same diode circuit, Figure 4.4, which shows that at instant \( t \), when valve 3 becomes forward biased starts to conduct with valve 1 carrying the full dc current. The conducting of both valves 1 and 3 represents a short circuit between phases a and b with the short-circuit current rising from phase b through valve 3 into phase a through valve 1. But once the short-circuit current equals the dc current through valve 1, its net current reaches zero, valve 1 stops conducting and the commutation is complete. The short-circuit current between the two phases for this period of commutation, angle \( \gamma_0 \), is defined by
Figure 4.4 Three-phase, full-wave diode converter operation, including commutation angle: (a) six-pulse diode converter; (b) voltage and current waveforms.

\[ 2L \frac{di}{dt} = \sqrt{2} E \sin \omega t \]

where \( L \) is the inductance of each phase (neglecting resistance). Integration gives

\[ i_r = \frac{E}{\sqrt{2} \omega L} (1 - \cos \omega t) \]
Assuming that when $I_a = I_d$, $\omega t = \gamma_0$ gives

$$I_d = \frac{E}{\sqrt{2\omega L}} (1 - \cos \gamma_0) \quad \text{(4.5)}$$

From (4.5) the commutation angle $\gamma_0$ can be calculated.

It is noted from Figure 4.4, that the output voltage is somewhat reduced compared to the output voltage corresponding to $\gamma = 0$ in Figure 4.3. During commutation the output follows the mean of the two short-circuited voltages. The lost voltage corresponds to the shaded area every 60 degrees and is given by

$$\partial V = \partial A/\sqrt{3}$$

$$\partial A = \frac{1}{2} \int_0^{\pi} \sqrt{2} E \sin \omega t d(\omega t) = \frac{1}{\sqrt{2}} E (1 - \cos \gamma_0) \quad \text{(4.6)}$$

$$\partial V = \frac{3}{\sqrt{2\pi}} E (1 - \cos \gamma_0)$$

$$\partial V = \frac{3\omega L}{\pi} I_d \quad \text{(4.7)}$$

$$V_d = V_0 - \partial V = V_0 - \frac{3\omega L}{\pi} I_d$$

Thus the dc voltage drop in the converter due to the commutation of dc current $I_d$ is directly proportional to $I_d$. On the dc side the voltage drop may be simulated as a resistance, equal to $3\omega L/I_d$. This does not mean that there is a loss of power, because it is not an actual resistance. It can be visualized from the current waveform in Figure 4.4 that the current is somewhat shifted to the right by the commutation process. This means that the ac side power factor is reduced from unity to a somewhat lower value in the lagging direction, which in turn means that some reactive power is consumed. This power factor reduction corresponds to the reduction in the dc voltage.

Equating the dc and ac power

$$\sqrt{3} EI \cos \phi = V_d I_d = \left( V_0 - \frac{3\omega L}{\pi} I_d \right) I_d \quad \text{(4.8)}$$

which, combined with (4.1) and (4.3) gives

$$\cos \phi = 1 - \frac{1}{\frac{V_0}{3\omega L}} \frac{3\omega L}{\pi} \quad \text{(4.9a)}$$

For practical estimation, power factor angle $\phi$ may be taken as

$$\phi = \alpha + 2\gamma/3, \quad \text{for} \quad 0 < \alpha < 30^\circ$$

$$\phi = \alpha + \gamma/3, \quad \text{for} \quad 30^\circ < \alpha < 90^\circ \quad \text{(4.9b)}$$

### 4.3 THYRISTOR-BASED CONVERTER (with gate turn-on but without gate turn-off)

#### 4.3.1 Rectifier Operation

From the discussions on the diode rectifier, it is easy to recognize that if the devices had a turn-on control, the start of each commutation could be delayed and hence the output voltage reduced or even reversed at will.
Consider again the diode voltage waveform of Figure 4.4 when from instant $t_3$ valve 3 becomes forward biased and it is ready to commutate current from valve 1. This start of commutation could be delayed if the devices were thyristors. Figure 4.5 shows the output dc voltage and phase-current waveforms for the commutations delayed by an angle $\alpha$. The short-circuit current of the commutation process is now defined as before by

$$2L\frac{di}{dt} = \sqrt{2} E \sin \omega t$$
Assuming now that the start of commutation is at $\omega t = \alpha$, integration for $\omega t = \alpha$ and $I_x = 0$, gives

$$i_x = \frac{E}{\sqrt{2} \omega L} \cos \alpha - \cos \omega t$$

and when $\omega t + \gamma$, $I_x = i_x$, gives

$$I_x = \frac{E}{\sqrt{2} \omega L} \left[ \cos \alpha - \cos (\alpha + \gamma) \right] \quad \text{(4.10)}$$

From (4.10), angle $\gamma$ can be calculated for a given value of angle $\alpha$. It is seen that angle $\gamma$ decreases with increase in angle $\alpha$. This should be obvious since the rate or rise of short-circuit current is greater with increase in the short-circuited voltage.

Equation for the dc output voltage can be obtained by first calculating the output voltage with commutation angle $\gamma = 0$, and then subtracting the voltage lost due to commutations. With $\gamma = 0$, the output voltage, taking a 60 degree segment, is defined by

$$V_d = \frac{3}{\pi} \int_{\alpha}^{\alpha+\gamma} \sqrt{2} E \cos \omega t \, d(\omega t)$$

$$V_d = \frac{3\sqrt{2}}{\pi} E \cos \alpha = V_0 \cos \alpha \quad \text{(4.11)}$$

where $V_0$ is the output voltage corresponding to $\alpha = 0$ and $\gamma_0 = 0$. Thus the output voltage with $\gamma_0 = 0$ decreases as the cosine function of $\alpha$. This means that with increasing $\alpha$, the output voltage decreases slowly first reaching 86.6% for $\alpha = 30$ degrees, 50% with $\alpha = 60$ degrees and 0 at $\alpha = 90$ degrees, and negative for $\alpha > 90$ degrees.

Now taking into account the commutation angle, the area under each commutation is given by

$$\delta A = \frac{1}{2} \int_{\alpha}^{\alpha+\gamma} \sqrt{2} E \sin \omega t \, d(\omega t) = \frac{1}{\sqrt{2}} E (\cos \alpha - \cos (\alpha + \gamma))$$

This area represents dc voltage drop every 60 degrees, therefore,

$$\delta V = \frac{3}{\sqrt{2} \pi} E \left[ \cos \alpha - \cos (\alpha + \gamma) \right] \quad \text{(4.12)}$$

and

$$V_d = V_0 \cos \alpha - \delta V$$

$$= \frac{V_0}{2} \left[ \cos \alpha + \cos (\alpha + \gamma) \right] \quad \text{(4.13)}$$

or $V_d/V_0$, the per unit voltage is given by

$$\frac{V_d}{V_0} = \frac{1}{2} \left[ \cos \alpha + \cos (\alpha + \gamma) \right] \quad \text{(4.14)}$$

From (4.11) and (4.12),

$$\delta V = \frac{3 \omega L}{\pi} I_x$$

which gives
Section 4.3 Thyristor-Based Converter (with gate turn-on but without gate turn-off)

4.3.1 Thyristor-Based Converter

(4.13) and (4.14) have been used to calculate the power factor and the voltage drop for commutation, respectively. Now, we will consider the effect of the delay angle on the converter output voltage.

As would be expected, the voltage drop for commutation is the same \((3\omega L/\pi)I_d\) for any delay angle; i.e., the commutation voltage integral is always the same for the same current.

Thus a converter output voltage for any value of delay angle \(\alpha\), dc current \(I_d\), and ac voltage \(E\) can be obtained from (4.15) and is represented by a simple equivalent circuit of a variable dc source in series with an equivalent resistor as shown in Figure 4.6. This resistor in turn is a reflection of reduced lagging reactive power on the ac side.

In per unit terms, assuming \(V_{on}\) as 1 pu \(V_0\), inductance \(\omega L\) in per unit as \(X_p = (\omega L \times I)/(E/\sqrt{3})\), then combining (4.3) and (4.15) gives a per unit value of the dc output voltage:

\[
V_d/V_{on} = \cos \alpha - \frac{X_p}{2}
\]  

(4.16)

Given, say, converter transformer plus the system impedance is 20% and inductive, (0.2 pu), the dc voltage will drop by about 10% from no load to full load, and the power factor on the ac side will drop correspondingly.

If it is assumed that \(V_d = V_0 \cos \phi\), then the power factor \(\cos \phi\) is approximately given by

\[
V_d/V_0 = \cos \phi = \cos \alpha - \frac{3\omega L}{\pi} I_d = 1/2 [\cos \alpha + \cos(\alpha + \gamma)]
\]  

(4.17)

4.3.2 Inverter Operation

Consider first, converter operation assuming zero commutation angle; Figure 4.7 shows the output voltage with varying delay angle.

Figure 4.7(a) is for the normal rectifier operation with a small delay angle \(\alpha\) and shows the positive output voltage by inclined hatched areas. Figure 4.7(b) is for the case when delay angle \(\alpha\) is increased beyond 60 degrees and it is seen that there are some negative areas corresponding to the angle in excess of 60 degrees, shown by horizontal hatching. If the dc load on the rectifier was resistive, its operation would be discontinuous because conduction would not occur in the negative direction. But with a large inductor, the difference between the positive and negative areas will average out to a resultant output voltage on the dc side.

At 90 degrees delay, the positive and negative voltage areas become equal and the average voltage is zero as per (4.11).
Figure 4.7 Converter operation at different angles of delay (assuming zero commutation angle).
\[ V_d = V_0 \cos 90^\circ = 0 \]

As the delay angle is further increased, the average voltage becomes negative and at 180 degrees the negative voltage becomes as large as that for the rectifier with zero delay angle.

It is assumed that for an inverter to operate and feed active power into the ac system, there is another source of dc power which causes the dc current to flow in the same direction, against the converter's dc output voltage, thus feeding dc power into the inverter.

Actually, an inverter can not be operated at a delay angle of 180 degrees, because some time (angle \( \gamma \)) is needed for the commutation of current and further time (angle \( \delta \)) is needed for the outgoing valve to fully recover (turn-off) before the voltage across it reverses and becomes positive. Otherwise the outgoing valve will commutate the current back and lead to a fault known as commutation failure (discussed later).

Figure 4.8 shows inverter operation with an angle \( \alpha \), which is somewhat less than 180 degrees. Also shown are the valve currents and various angles, dividing the range of 180 degrees angle into the delay angle \( \alpha \), commutation angle \( \gamma \), safe turn-off angle \( \delta \), and angle of advance \( \beta = \gamma + \delta \). For safe operation, angle \( \delta \) must not be less than \( \delta _0 \). Often for convenience, inverter equations are referred to in terms of angle of advance \( \beta \), commutation angle \( \gamma \), and margin angle \( \delta \). All the equations derived earlier in terms of \( \alpha \) and \( \gamma \) still apply, and if preferred they can be obtained by substituting \( \alpha \) with \( \pi - \beta \) or \( \pi - (\gamma + \delta) \); they are not included here.

Figure 4.9 shows the phasor diagram of ac voltage and current, indicating the range of operation of a line-commutating converter with the hatched area. It shows that the operation is limited to two quadrants; the rectifier operation limited by the commutation requirements at \( \alpha = 0 \), and the inverter operation limited at the other end by the commutation and valve recovery requirements. Throughout the range it consumes reactive power, which can be calculated from (4.9) and (4.17) for the power factor. For a given current and voltage, the active power decreases and reactive power increases, with increase in \( \alpha \) from zero until it reaches 90 degrees-(\( \gamma/2 \)) when the dc output voltage reduces to zero. At this point the active power is zero and the reactive power is at its maximum. In fact, a line-commutating converter is also used as a static var compensator to consume controlled reactive power. This is done by operating the converter with a short circuit through a dc inductor on the dc side and controlling the dc current flow by controlling angle \( \alpha \).

It should be noted that the equations above represent the rectifier and inverter conditions for commutation angle \( \gamma \) less than 60 degrees; if this angle is exceeded, the operation is no longer represented by the same equations since two commutations will take place simultaneously. This situation is not likely in steady-state conditions but may occur during high dc fault current. It should also be noted that operation with delay angle \( \alpha \) less than 30 degrees and commutation angle \( \gamma \) greater than 60 degrees simultaneously is not possible. If for, say, \( \alpha = 0 \), the current is so increased that the corresponding angle \( \gamma \) is greater than 60 degrees, then the firing of the valves will not take place at \( \alpha = 0 \) but will be automatically delayed so that \( \gamma = 60^\circ \). This situation continues until \( \alpha = 30^\circ \) and then \( \gamma \) can be increased. Under such conditions, the equivalent commutation resistance in (4.15) and Figure 4.6 become \( 9 \omega L/\pi \), three times the normal value of \( 3 \omega L/\pi \).
4.3.3 Valve Voltage

Figure 4.10 shows the valve voltage, valve 5 for example, during inverter operation. The upper waveforms show the ac voltage, valve sequence, and the voltages during commutations. As explained before, the commutations are enabled by short circuits between phases. During these short circuits the voltage of the two short-circuited ac phases follow the mean of the respective two phases. Diagram for valve 5 voltage shows that during conduction period of $120^\circ + \gamma$, the voltage is zero, and
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\[ \alpha = \pi - (\delta_0 + \gamma) \]
\[ \phi = \delta_0 + \frac{2\gamma}{3} \]
\[ \alpha = 0 \]
\[ \phi = \frac{2\gamma}{3} \]

Figure 4.9 Operation zone of thyristor-based converter.

\[ \alpha = \left( \frac{\pi}{2} - \frac{\gamma}{2} \right), \ \phi = \frac{\pi}{2} \]

Figure 4.10 Voltage across a valve in a thyristor converter: (a) converter operation as an inverter; (b) voltage across valve 5.
at the end of commutation from valve 5 to valve 1, the voltage jumps to a negative value corresponding to the voltage $v_{ca}$. As mentioned before, the duration of this negative voltage needs to be sufficient for valve 5 to recover before the voltage goes positive. As the valve voltage follows voltage $v_{ca}$, it is distorted by change in the voltage $v_{ca}$ during short circuit of phases b and c for commutation from valve 6 to valve 2. Following that it is again distorted by the change in voltage $v_{ca}$ during commutation from valve 1 to valve 3; however, at the completion of this commutation, the valve voltage follows the voltage $v_{cb}$, which is later distorted by commutation from valve 2 to valve 4. The cycle is complete when valve 5 turns on again. Thus the voltage across valve 5, connected to phase c, follows the voltage waveforms, $v_{ca}$ and $v_{cb}$. Similarly the voltage across valve 2, the other valve connected to phase c, follows the voltage waveforms $v_{xc}$ and $v_{bc}$, and so on. During the inverter operation the valve voltage is positive much of the time and obviously during rectifier operation it will be negative much of the time. Given the circuit inductances and capacitances, there will be a voltage overshoot at each voltage jump, resulting in higher valve voltage when the overshoot is during the peak of the valve voltage. It is therefore necessary to provide R-C damping circuits across the valve devices.

4.3.4 Commutation Failures

It was mentioned earlier that a safe minimum angle of advance $\beta$ is needed in order to allow successful commutation of current (angle $\gamma$) and for the outgoing valve to fully recover (angle $\delta > \delta_b$) before the voltage across it reverses and becomes positive. Otherwise the outgoing valve will commutate the current back and lead to a fault known as commutation failure. On one hand it is desirable to minimize the angle $\beta$ when it is necessary to maximize the inverter output voltage; on the other hand, allowance has to be made for current rise and/or reduction of ac system voltage just before and during the commutation process. Some allowance has to be made for reasonable events and then it has to be accepted that some commutation failures will still occur on some statistical basis and provide for a safe ride through.

Referring to Figure 4.11, $t_1$ is the point where valves 1 and 2 are conducting, valve 3 turns on, and commutation from valve 1 to valve 3 is expected to take place. Suppose the commutation fails to complete by point $t_2$ the point of voltage crossing. The commutation will reverse, as shown, and valve 1 together with valve 2 will continue to carry the dc current. Consequently the dc voltage continues to fall as per voltage $v_{ca}$. Then at point $t_3$ valve 4 turns on to take over the current from valve 2, at which time $v_{ca}$ is short circuited and the dc voltage falls to zero. Now assuming that the commutation from valve 2 to valve 4 is successful, the dc current is effectively bypassed through the phase-leg of valves 1 and 4. Following that, valve 5 has no chance to take back the current, because its voltage is reverse biased. The dc short circuit ends $t_4$ when valve 6 takes the current over from valve 4, with the dc voltage going slightly negative first and the converter continues to function correctly. This type of commutation failure is referred to as a single commutation failure.

When a commutation failure occurs, the scenario is more likely to end with a single commutation failure, given that the dc inductor is large enough to limit the rate of rise of current and the protective means advance the turn-on of the next valve with detection of a commutation failure. Again there is no guarantee that the commutation of the next valve, immediately after the commutation failure, will be successful. In the example above if the commutation from valve 2 to valve 4 also fails to complete,
Figure 4.11 Commutation failure in a thyristor-based line-commutated converter: (a) six-pulse thyristor converter; (b) inverter voltage during a single commutation failure; (c) inverter voltage during double commutation failure.
then the dc output voltage will go through a full ac cycle voltage $v_{ca}$, following that if all else is well, the normal operation will continue.

In general this problem is quite manageable in power systems as is evident from a large number of HVDC projects in satisfactory operation.

### 4.3.5 AC Current Harmonics

Neglecting commutation angle, the current is made up of 120 degree pulses as shown in Figure 4.12(a). Analysis of ac current can be obtained by Fourier analysis and is given by

$$i_n = \frac{2\sqrt{3}}{\pi} I_d \left[ \cos \omega t - \frac{1}{5} \cos 5\omega t + \frac{1}{7} \cos 7\omega t - \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t - \cdots \right]$$

(4.18)

The harmonics are of the order of $6k \pm 1$, where $k$ is an integer. The rms value of any term in (4.18) is given by

$$I_n = I_d \frac{\sqrt{6}}{n\pi}$$

(4.19)

With $n = 1$, the rms value of the fundamental is given by

$$I_1 = \frac{\sqrt{6}}{\pi} I_d = 0.78 I_d$$

(4.3)

Assuming 1:1 ratio of a wye/wye transformer, if a delta/wye transformer with $\sqrt{3}$:1 ratio is adopted, the secondary voltages of this transformer would be displaced.

Figure 4.12 Six-pulse and 12-pulse current-sourced converters: (a) six-pulse wye/wye circuit and current waveform; (b) six-pulse wye/delta circuit and current waveform; (c) twelve-pulse circuit and current waveform.
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by 30 degrees with respect to the corresponding voltages in a wye/wye transformer. The line current will now be as shown in Figure 4.12(b). The analysis will show that the harmonics are defined by the same (4.16) above, except that harmonics of the 5th, 7th, 17th, 19th, 29th, etc. orders are of opposite sign.

When two six-pulse converters of equal capacity, one with wye/wye transformer of ratio 2:1, and the other with delta/wye transformer of ratio $2\sqrt{3}:1$, are connected together in either series or parallel, the resultant current is given by

$$i_n = \frac{2\sqrt{3}}{\pi} I_d \left[ \cos \omega t - \frac{1}{11} \cos 11 \omega t + \frac{1}{13} \cos 13 \omega t - \frac{1}{23} \cos 23 \omega t + \cdots \right]$$  (4.20)

This equation represents the ac current of a 12-pulse converter and has a waveform shown in Figure 4.12(c). Harmonics of the orders 5th, 7th, 17th, 19th, ..., which do not enter the ac system, will circulate between the two six-pulse converters. The harmonics are of the order of $12k \pm 1$, where $k$ is an integer. In fact a 12-pulse converter will often have one transformer with one primary and two secondaries. It follows that one can have a 24-pulse converter by combining four six-pulse converters, with 15 degrees phase-shift obtained with phase-shifting transformers.

The equations above took no account of commutation angle. However, it is important to consider the commutation angle because the harmonics decrease considerably. If this is considered, the current wave shape for analysis can be defined in three parts as in Figure 4.13.

$$i_p = I_d \frac{(\cos \alpha - \cos \omega t)}{[\cos \alpha - \cos (\alpha + \gamma)]}$$

for

$$\alpha < \omega t < (\alpha + \gamma)$$

$$I_q = I_d$$

for

$$(\alpha + \gamma) < \omega t < [(2\pi/3) + \alpha].$$

$$i_r = I_d - I_d \frac{\cos \alpha - \cos (\omega t - 2\pi/3)}{[\cos \alpha - \cos (\alpha + \gamma)]}$$

for

$$[(2\pi/3) + \alpha] < \omega t < [(2\pi/3) + \alpha + \gamma].$$

Based on Fourier analysis of the waveform defined above, Figures 4.14 to 4.19 show curves of the harmonic current $I_n$ as percentage of the fundamental $I$ (defined by equations above), against the commutation angle $\gamma$ for different values of $\alpha$ or $\delta$ for the 5th, 7th, 11th, 13th, 17th, and 19th in order to convey the nature of these curves. Curves for specific values of the delay angle $\alpha$ and the margin angle $\delta$ are the same, because $\delta$ is a mirror image of $\alpha$.

It is seen from these curves that, as $\gamma$ increases, the magnitude of harmonics decreases, and with higher orders decreases more rapidly. Each harmonic decreases to a minimum at an angle $\gamma = 360^\circ/n$ and then rises slightly thereafter. It is worth noting that for practical purposes $\gamma$ will likely be in the range of 15 to 30 degrees at full load.

Obviously the voltage harmonics on the ac system side are a function of the ac system impedance for each harmonic current injected into the system by the converter.
Chapter 4 ■ Self- and Line-Commutated Current-Sourced Converters

Figure 4.13 DC current and voltage waveform definition for harmonic analysis.

Figure 4.14 Variation of 5th harmonic current in relation to angle of delay \( \alpha \) (or margin angle \( \delta \)) and commutation angle \( \gamma \).
Figure 4.15 Variation of 7th harmonic current in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$.

Figure 4.16 Variation of 11th harmonic current in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$. 
Figure 4.17 Variation of 13th harmonic current in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$.

Figure 4.18 Variation of 17th harmonic current in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$. 
**Figure 4.19** Variation of 19th harmonic current in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$. 
4.3.6 DC Voltage Harmonics

On the dc side of a converter, the output voltage is of a form, which depends on the pulse order, angle of delay $\alpha$, and angle of commutation $\gamma$. The output voltage consists of a dc voltage, on which are superimposed a number of harmonics; these have an order $n$ equal to $kp$, where $k$ is an integer and $p = 6$ for a six-pulse converter. With zero delay angle, and no load or neglecting commutation angle, the rms amplitude of each harmonic is given by

$$V_n = V_0 \frac{\sqrt{2}}{n^2 - 1} \quad (4.21)$$

Thus sixth harmonic has an amplitude of 4.04%, twelveth harmonic has amplitude of 0.99% of the fundamental dc voltage, etc., for zero delay and commutation angles.

With reference to Figure 4.13(a), for harmonic analysis with an angle of delay $\alpha$ and commutation angle $\gamma$, the 60 degree segment of the dc voltage waveform can be defined in three parts:

$$e_\alpha = \sqrt{2} E \cos \left( \omega t + \frac{\pi}{6} \right) \quad \text{for} \quad 0 < \omega t < \alpha$$

$$e_\gamma = \frac{1}{2} \left[ \sqrt{2} E \cos \left( \omega t - \frac{\pi}{6} \right) + \sqrt{2} E \cos \left( \omega t + \frac{\pi}{6} \right) \right] \quad \text{for} \quad \alpha < \omega t < (\alpha + \gamma) \quad (4.22)$$

$$e_\delta = \sqrt{2} E \cos \left( \omega t - \frac{\delta}{6} \right) \quad \text{for} \quad (\alpha + \gamma) < \omega t < (\pi/3)$$

Figures 4.20, 4.21, and 4.22 show characteristics of harmonics as per unit of the ideal dc voltage $V_0$ against the commutation angle $\gamma$, for different values of delay angle $\alpha$ for 6th, 12th, and 18th harmonic, respectively. It is seen from these characteristics that:

- For small values of angle $\gamma$, the harmonic magnitudes increase with the increase in angle $\alpha$ and the higher the harmonics, the more rapid the increase.
- For a constant angle $\alpha$, the harmonics decrease (they may increase slightly at first for small angles $\alpha$) and reach a first minimum at, approximately, $\gamma = \pi/n$.
- For $\gamma = \pi/(n + 1)$ and $\gamma = \pi/(n - 1)$, the harmonics are constant for any angle $\alpha$.
- At $\gamma = 2\pi/n$, there is a maximum and at $\gamma = 3\pi/n$ there is a further minimum.

When two six-pulse converters, one with wye/wye transformer and the other with wye/delta transformer, are connected in series to form a 12-pulse converter, the harmonics that are of the orders that are odd multiples of 6, (6th, 18th, 30th . . .), will be equal and opposite in phase and cancel out, where as harmonics of the orders that are even multiples of 6, (12th, 24th, 36th . . .) will be in phase.

Obviously the current harmonics on the dc side are a function of the dc side impedance for each harmonic voltage produced by the converter.
Figure 4.20 Variation of 6th harmonic voltage in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$. 
Figure 4.21 Variation of 12th harmonic voltage in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$. 
4.4 CURRENT-SOURCED CONVERTER WITH TURN-OFF DEVICES (current-stiff converter)

A current-sourced converter with turn-off devices is also referred to as current-stiff converter. As mentioned previously, these turn-off devices must have reverse withstand voltage capability (symmetric devices) or have diodes in series if they are asymmetric devices.

In the current-sourced converter with conventional thyristors discussed above, operation of the converter is limited to the third and fourth quadrant (lagging power factor). This is because thyristors do not have turn-off capability and the dc current has to be commutated from one valve to another while the anode-cathode voltage of the incoming valve is still positive. Also, such a converter needs an ac voltage source for commutation.

In the voltage-sourced converters discussed in Chapter 3, there is the dc capacitor, which facilitates rapid transfer of current from an outgoing turn-off valve to the opposite valve in a phase-leg, irrespective of the direction of the ac current. The capacitor is assumed to be large enough to handle alternate charging and discharging

Figure 4.22 Variation of 18th harmonic voltage in relation to angle of delay $\alpha$ (or margin angle $\delta$) and commutation angle $\gamma$. 

\[ \frac{V_{18}}{V_0} \]
without substantial change in dc voltage. With turn-off capability, the valves can be
turned off at will. However, turn-off devices in order to turn off still require an
alternate path for rapid transfer of current. Otherwise, they will have to dissipate a
large amount of energy to turn off current in an inductive circuit. It can be visualized
that if ac capacitors are placed between phases, on the ac side of the valves, Figure
4.23(a), they can facilitate rapid transfer of current from the outgoing turn-off valve
to the incoming valve.

Commutation of current from valve 1 to valve 3 is illustrated in Figure 4.23(b). Given
low inductance of the ac shunt capacitor and the bus connections, the transfer
(commutation) is rapid and there is no commutation angle to speak of as far as the
valves are concerned. Actually, with due respect to the turn-on di/dt limit of the
devices, inductance of the capacitors and the bus connections can be duly exploited.
Also it is to be noted, that when a valve turns off, valve 1 in Figure 4.23(b), its rate
of rise of voltage is cushioned by the ac capacitor. Details of turn-on and turn-off in
a few tens of microseconds time frame of the commutation is not discussed here.
Suffice it to say that it is a complex and important matter in terms of device losses
and snubber requirements. These capacitors need to handle a sustained alternating
charge/discharge current of the converter valves.

Unlike the line commutated converter using conventional thyristors, this con-
verter with turn-off valves can operate even with a leading power factor and it does
not need a pre-existing ac voltage for commutation. It can in fact operate as an inverter
into a passive or an active ac system.

Figure 4.23(c) shows the anode-bus current connected to the anode side of valves
1, 3, and 5 and transfer of this incoming dc current from valve 1 to 3, to 5, to 1 etc.,
in a closed three-valve sequence in a three-phase converter. Similarly shown are the
cathode bus current, the outgoing dc current, and how it transfers from valve 2 to 4,
to 6, to 2 etc., in a closed three-valve sequence. The two sequences are phase shifted
by 60 degrees and they together form a three-phase, full-wave bridge converter.
Consequent injected ac current in the three phases is also shown in Figure 4.23(c),
which is same as for the conventional thyristor converter when neglecting commutation
angle, Figure 4.3(b). The currents are injected without the support of ac system volt-
ages, and therefore, the phase angle and the frequency of this injected ac current can
be controlled.

To understand the operation of this converter, it is appropriate to visualize it as
an ac current generator connected to an ac system, which is front-ended with ac
capacitors [Figure 4.23(d)]. In FACTS applications, the interface beyond the ac capaci-
tor is likely to be a transformer which may be followed by ac system and filters to
limit the harmonics from entering the ac system. The ac voltage at the converter
terminal is the result of the interaction of the converter-generated ac current with the
ac system impedance and the system voltage. Naturally, the injected current has to
be coordinated with the characteristics of the ac system in terms of its frequency and
phase relationship to ensure that the consequent ac voltages are acceptable.

In the context of shunt-connected FACTS Controllers, this converter will simply
inject an ac current into the system with the necessary ac voltage to force such an
injection of current. This assumes of course that the dc current source is capable of
driving such a current.

In the context of series-connected FACTS Controllers, the ac current in the line
would flow through the valves to become a unidirectional dc current. Depending on
the dc side impedance and the source, dc voltage of either polarity would appear.
This dc voltage is reflected back as the converter ac voltage, which in turn will influence
Section 4.4 ■ Current-Sourced Converter with Turn-Off Devices (current-stiff converter)

Figure 4.23 Self-commutating current-sourced converter: (a) six-pulse converter; (b) commutation process; (c) current waveforms; (d) system interface.
the line current. If for some reason the connection to the ac systems becomes open, the converter is blocked, the current bypassed by the valves and the dc side voltage can be quickly reversed to manage the bypassed current; this is a normal practice in HVDC.

Since the current waveform of this single six-pulse converter is identical to that of Figure 4.3(b), the harmonic content is given by (4.18). The harmonics are of the order of $6k \pm 1$, where $k$ is an integer. The rms value of any term in (4.18) is given by (4.19) and the rms value of the fundamental is given by (4.3).

Two six-pulse converters of equal capacity, one with wye/wye transformer and the other with wye/delta transformer, or one transformer with two secondaries, one wye connected and the other delta connected, will result in a 12-pulse converter with harmonics defined by (4.20). The ac side fundamental and harmonic voltages are a function of the ac system and the injected current.

A dc side converter voltage will also have harmonics. Assuming sinusoidal voltage at the ac capacitor terminals, the dc voltage harmonics are defined by (4.22), but with $\gamma = 0$:

$$
e_i = \sqrt{2} E \cos \left( \omega t + \frac{\pi}{6} \right) \quad \text{for} \quad 0 < \omega t < \alpha$$

$$
e_u = \sqrt{2} E \cos \left( \omega t - \frac{\pi}{6} \right) \quad \text{for} \quad \alpha < \omega t < (\pi/3)$$

The per-unit values of these harmonics are given by the values on the Y-axis of Figures 4.20, 4.21, and 4.22, for the 6th, 12th, and 24th harmonics.

Various PWM concepts discussed for the voltage-sourced converters in Chapter 3 are applicable to the current-sourced converters, although they are not discussed here. An advantage of the PWM operation is that the commutation capacitor size will decrease.

### 4.5 CURRENT-SOURCED VERSUS VOLTAGE-SOURCED CONVERTERS

There are some advantages and disadvantages of current-sourced versus voltage-sourced converters:

- Diode-based converters are the lowest cost converters, if control of active power by the converter is not required.
- If the leading reactive power is not required, then a conventional thyristor-based converter provides a low-cost converter with active power control. It can also serve as a controlled lagging reactive power load (like a thyristor-controlled reactor).
- The current-sourced converter does not have high short-circuit current, as does the voltage-sourced converter. For current-sourced converters, the rate of rise of fault current during external or internal faults is limited by the dc reactor. For the voltage-sourced converters, the capacitor discharge current would rise very rapidly and can damage the valves.
- The six-pulse, current-sourced converter does not generate third harmonic voltage, and its transformer primaries for a 12-pulse converter do not have to be connected in series for harmonic cancellation. It is also relatively simple to obtain a 24-pulse operation with phase-shifting windings.
In a current-stiff converter, the valves are not subject to high $dv/dt$, due to the presence of the ac capacitors.

Ac capacitors required for the current-stiff converters can be quite large and expensive, although their size can be decreased by adoption of PWM topology. In general the problem of a satisfactory interface of current-sourced converters with the ac system is more complex.

Continuous losses in the dc reactor of a current-sourced converter are much higher than the losses in the dc capacitor. These losses can represent a significant loss penalty.

With the presence of capacitors, which are subjected to commutation charging and discharging, this converter will produce harmonic voltages at a frequency of resonance between the capacitors and the ac system inductances. Adverse effects of this can be avoided by sizing the capacitors such that the resonance frequency does not coincide with characteristic harmonics.

These harmonics as well as the presence of a dc reactor can result in overvoltages on the valves and transformers.

Widespread adoption of asymmetrical devices, IGBTs and GTOs, as the devices of choice for lower on-state losses, has made voltage-sourced converters a favorable choice when turn-off capability is necessary. The device market is generally driven by high-volume industrial applications, and as a result symmetrical turn-off devices of high-voltage ratings and required operating characteristics, in particular the switching characteristics, may not be readily available until the volume of the FACTS market increases. However as the devices evolve, particularly with the evolution of advanced GTOs discussed in Chapter 2, it is important to continuously re-evaluate the converter topology of choice.

**REFERENCES**


